

ASSIGNMENT 6: ADDER AND SUBTRACTOR

1. Implement $F = \sum(1,3,7,11,15)$ with don't care condition $d = \sum(0,2,5)$
2. With logic diagram and function table explain the operation of 4 to 1 line multiplexer.
3. With logic diagram and truth table explain the working of 3 to 8 line decoder.
4. Design a full adder circuit using decoder and multiplexer.
5. Explain full-adder & half-adders
6. Design a full-adder with two half-adders and an OR gate.
7. Explain Magnitude Comparator.

