AMIRAJ

COLLEGE OF ENGINEERING & TECHNOLOGY

LABORATORY MANUAL

DIGITAL FUNDAMENTALS

SUBJECT CODE: 3130704

DEPARTMENT OF COMPUTER ENGINEERING

B.E. 3rd SEMESTER

NAME:_____
ENROLLMENT NO: _____
BATCH NO: _____
YEAR: _____

Amiraj College of Engineering and Technology,
Nr.Tata Nano Plant, Khoraj, Sanand, Ahmedabad.

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COLLEGE OF ENGINEERING & TECHNOLOGY

Amiraj College of Engineering and Technology,

Nr.Tata Nano Plant, Khoraj, Sanand, Ahmedabad.

CERTIFICATE

This is to certify that Mr. / Ms. _____

Of class_____ Enrolment No _____has

Satisfactorily completed the course in _____as

by the Gujarat Technological University for ____ Year (B.E.) semester___ of

Mechanical Engineering in the Academic year_____.

Date of Submission:-

Faculty Name and Signature

(Subject Teacher)

Head of Department

(COMPUTER)

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LIST OF EXPERIMENTS

Sr. No.	Title	Date of Performance	Date of submission	Sign	Remark
1.	To implement Basic gates with the help of NAND and NOR gates				
2.	To design and implement a Half adder, Half subtractor circuits				
3.	To design and implement a full adder, full subtractor circuits.				
4.	A) To verify the truth table of MUX and DEMUX. B) To implement 3 X 8 Decoder and 8 X 3 Priority Encoder C) To Design And Implement SR,JK Flipflop Using Gates				
5.	To Study BCD to gray and gray to BCD code converter.				
6.	To Study 4-bit Comparator.				
7.	To Study De morgon's Law				
8.	To implement 4-bit Universal Shift Register.				
9.	Realization of 4-bit Synchronous up and down counter design.				
10.	Realization of Decade counter.				

PRACTICAL NO:-1

AIM: To implement Basic gates with the help of NAND and NOR gates

APPARATUS:

THEORY: The basic building block o digital systems are known as gates because they Control the passage of signals. Gate is digital circuit with one or more input but only one output. The gates by use of which the work of other gates can be performed are known as "Universal gates". NAND and NOR gates are universal gates.

We can define the Gates as follows:

AND gate: The output is high when all the inputs are high.

OR gate: The output is high when either of the input is high.

NOT gate: The output is not equal to input.

NAND gate: Its output is compliment of AND gate.

NOR gate: Its output is compliment of OR gate.

XOR gate: Its output is high if either of the inputs is high.

XNOR gate: Its output is compliment to that of output of XOR.

NAND GATE AS UNIVERSAL GATE:

NOR GATE AS UNIVERSAL GATE:

CONCLUSION:

PRACTICAL NO:- 2

AIM: To design and implement a Half adder, Half subtractor circuits

APPARATUS:

THEORY: Digital computers perform variety of tasks involving processing tasks.

A combinational circuit the addition of two bits without taking into account previous carry is called half adder circuit.

A combinational circuit that performs subtraction of two bits without taking borrow is called a Half Subtractor.

LOGIC DIAGRAMS AND TRUTH TABLES:

(1) Half Adder

(2) Half Substractor

CONCLUSION:

PRACTICAL NO-3

AIM: To design and implement a full adder, full subtractor circuits.

APPARATUS:

THEORY: A combinational circuit the addition of three bits is called full adder circuit (2 significant bits and one end carry). The third input represents the carry from the lower previous significant position.

A combinational circuit that performs subtraction between two bits taking into account that "1" may be borrowed by a lower significant stage is called a full subtractor.

LOGIC DIAGRAMS AND TRUTH TABLES :

(1) Full Adder

(2) Full Substractor

CONCLUSION:

PRACTICAL NO:-4 (A)

AIM: - To verify the truth table of MUX and DEMUX.

APPERATUS: -

THEORY :- A MUX is a data selector. It is a logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output depends on selection line logic. In general there are 2^n i/p lines and n selection lines whose bit combinations determine which i/p is selected and 1 o/p.

A DEMUX is a data distributer. It is a logic circuit that distributes single data input to the available output depends on selection line logic. In general there are 2^n o/p lines and n selection lines whose bit combinations determine data distribution to a particular o/p line is selected and 1 i/p.

LOGIC DIAGRAMS AND TRUTH TABLES :

(1) MULTIPLEXER

(2) DEMULTIPLEXER

CONCLUSION:

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PRACTICAL NO:-4 (B)

AIM: - To implement 3 X 8 Decoder and 8 X 3 Priority Encoder

APPARATUS:

THEORY: A decoder accepts an *n* digit number as its "n" select" inputs and produces an output (usually a logic 0) at one of its 2^n possible outputs.

Decoders are usually referred to as n line to 2^n line decoders e.g. a 3 line to 8 decoder. In this type of decoder the selected output is set to logic 0, while all the other outputs remain at logic 1. Most of the decoders have an "enable" input $\bar{E}$ which "enable" the operation of the decoder. When $\bar{E}$ is set to 0, the device behaves as a decoder and selects the output determined by the select inputs. When the $\bar{E}$ input 1, the outputs of the decoder are all set to 1. (The bar over the E indicates that it is an "active low" input; that is, logic 0 enables the function).

The priority encoder is a logic circuit that responds to just one input in accordance with some priority system among all those that may be simultaneously high.

LOGIC DIAGRAM AND TRUTH TABLE:

CONCLUSION :

PRACTICAL NO:- 4 (C)

AIM: To Design And Implement SR,JK Flipflop Using Gates

APPARATUS:

THEORY:

S-R flip-flop:

In this flip flop we are using three inputs,they are S-R and clock input.Here we are making use of negative triggering i.e. flip-flop will be activated when the clock goes from '1' to '0' . Now, when both S-R input are same the output will remain in the previous state. When S=1 and R=0 ,flip-flop will be in set mode i.e. Q=1 and when R=1 and S=0 , it will be in reset mode i.e. Q=0.Now when both are 1, then basic definition of output is violated and consider the state as indeterminate .

JK flip flop:

This flip flop has five inputs and two outputs .The inputs are JK,CLK,preset and clear. The 2 outputs are complement of each other . This requires 4 ,3 i/p gates for implementation for the working of this flipflop the preset and clear should be at logic 1 .The JK flipflop IC 7476 is a negative edge triggered one .The state will change only when the clock pulse from 1 to 0 .

CIRCUIT DIAGRAM AND TRUTH TABLE:

1. S-R FLIP-FLOP:

2. JK FLIPFLOP:

CONCLUSION :

PRACTICAL NO :- 5

AIM:- To Study BCD to gray and gray to BCD code converter.

APPRATUS :-

THEORY :- The BCD code is Binary Coded Decimal code.It is a weighted code and is also sequential. It is less efficienft then binary codes, in the sense it requires more bits, e.g decimal number 14 can be represented as 1110 in binary but in BCD it is represented by 0001 0100.

The Gray code is a non weighted code. It is a cyclic code because successive codewords differs in one bit position only, i.e it is unit distance code. It is also called as reflective code.

LOGIC DIAGRAM AND TRUTH TABLE :-

CONCLUSION:

PRACTICAL NO :- 6

AIM:- To Study 4-bit Comparator.

APPRATUS :-

THEORY :- The 4-bit comparators basically compares two 4 bit numbers, and it gives o/p as two numbers are equal to each other or any one number is greater then the other one or any one number is less then the other.

LOGIC DIAGRAM AND TRUTH TABLE :-

CONCLUSION:-

PRACTICAL NO :- 7

AIM:- To Study De morgon's Law

APPRATUS :-

THEORY :- De-morgon's law represents two most powerful laws in Boolean Algebra

(i) (A+B)' = A'B'

(ii) (AB)' = A' + B'

LOGIC DIAGRAM AND TRUTH TABLE:-

CONCLUSION:

PRACTICAL NO:-8

AIM: To implement 4-bit Universal Shift Register.

APPARATURS:

THEORY: A Universal shift register is a bi-directional shift register , whose i/p can be either in serial form or in parallel form and whose o/p can be either in serial form or in parallel form. Basically A universal shift register is used to store digital data.

LOGIC DIAGRAM AND TRUTH TABLE:

CONCLUSION:

PRACTICAL NO:-9

AIM: - Realization of 4-bit Synchronous up and down counter design.

APPARATUS: -

THEORY: - This counter is used to count pulses in both direction up as well as down. Synchronous counters have advantages of high speed and less severe decoding problems. So synchronous counters have a single clock i/p to all flipflops and due to that they have higher operating frequencies then asynchronous counters.

LOGIC DIAGRAM , STATE DIAGRAM AND WAVEFORMS :-

CONCLUSION:-

PRACTICAL NO :- 10

AIM: - Realization of Decade counter.

APPARATUS: -

THEORY: - This counter is used to count pulses from 0 to 9. Sometimes it is called as BCD counter or divide by 10 counter. Since it is asynchrounous counter every output of the Flipflop is acting as a clock pulse for next Flipflop.

LOGIC DIAGRAM, STATE DIAGRAM AND WAVEFORMS:-

CONLUSION: