AMIRAJ
COLLEGE OF ENGINEERING & TECHNOLOGY

DEPARTMENT: ELECTRICAL

SEMESTER: 3RD

NAME: DIGITAL FUNDAMENTAL

CODE: 3130704

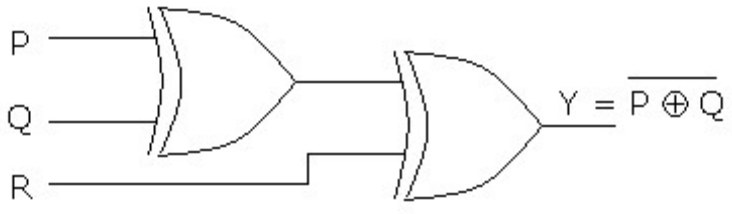
FACULTY NAME: SUNIL PATEL

QUESTION BANK

1. BINARY SYSTEMS AND LOGIC CIRCUITS

1 (A) BINARY SYSTEMS

1.	Do as directed**(May'15 NEW)** (i) Convert $(75)_{10}$ = (_____)$_2$ (ii) Convert $(101011)_2$ = (_____)$_{10}$ (iii) Convert $(10101101)_2$ = (_____)$_{16}$ = (_____)$_8$ (iv) What is self complementing code? Represent $(472)_{10}$ in 2421 self complementing code.	**06**
2.	Convert $(96)_{10}$ to its equivalent Gray code and EX-3 code.**(May'15 NEW) [IMP]**	**04**
3.	Perform addition in BCD format $(79)_{BCD}$ + $(16)_{BCD}$**(May'15 NEW) [IMP]**	**03**
4.	Perform subtraction of $(78)_{10}$ – $(58)_{10}$ using 2's complement addition method.**(May'15 NEW) [IMP]**	**03**
5.	Convert following numbers.**(May'15) [IMP]** (a) $(4021.2)_5$ = ( )$_{10}$. (b) $(B65F)_{16}$ = ( ) $_{10}$. (c) $(630.4)_8$ = ( ) $_{10}$. (d) $(41)_{10}$ = ( )$_2$	**07**
6.	Using 10's complement, subtract : $(72532-3250)_{10}$**(May'15) [IMP]** Using 10's complement, subtract : $(3250-72532)_{10}$ Using 2's complement, subtract : $(1010100-1000100)_2$	**07**
7.	Explain error detection codes and the reflected code with examples.**(May'15) [IMP]**	**07**
8.	Select the most appropriate option**(Dec'14 NEW) [IMP]** (i) Convert the decimal number 187 to 8-bit binary. (A) 10111011_2 (B) 11011101_2 (C) 10111101_2 (D) 10111100_2 (ii) Convert the binary number 1001.0010_2 to decimal. (A) 90.125 (B) 9.125 (C) 125 (D) 12.5 (vi) The 2's complement of the number 1101110 is (A) 0010001. (C) 0010010. (D) None.	**03**
9.	Answer the following questions**(Dec'14) [IMP]** 1. Add the two numbers $(A3E5)_{16}$ + ($CDA4)_{16}$	**02**
10.	1. Do subtraction using 12-bit two's complement addition method**(Dec'14) [IMP]** 27.125 – 79.625 2. Do BCD addition for given numbers 679.6 + 536.8	**07**
11.	Convert following 1. $(4E7.2)_{16}$ = $(?)_8$ 2. $(521.3)_8$ = $(?)_2$**(May'14) [IMP]**	**06**
12.	Write a brief note on Gray codes. Also discuss methods for conversion from gray to binary code and vice versa.**(May'14) [IMP]**	**07**
13.	Convert the following numbers as directed:**(Nov'13) [IMP]** (1) $(130)_{10}$ = ( )$_2$ (2) $(1011011)_2$ = ( )$_{10}$	**07**

	(3) $(1011101111)_2 = (\quad)_8$ (4) $(1101110111011111011)_2 = (\quad)_{16}$	
14.	Convert the decimal number 250.5 to base 3, base 4, base 7 and base 16.**(May'13) [IMP]/ (May'12) [IMP]**	**07/ 04**
15.	Convert the decimal number 250.5 to base 3, base 4, base 7, base 8 and base 16. **(Dec'12) [IMP]**	**14**
16.	Perform the subtraction with the following decimal numbers using 1's compliment and 2's compliments: (a) 11010-1101 , (b) 10010-10011**(May'13) [IMP]**	**07**
17.	Convert the decimal number 225.225 to binary, octal and hexadecimal.**(Dec'11) [IMP]/ (May'11) [IMP]**	**06/ 03**
18.	Represent the decimal number 8620 in BCD, Excess-3, and Gray code**(Dec'11) [IMP] / (May'11) [IMP]**	**03**
19.	Convert the following Numbers as directed:**(Dec'10) [IMP]** (1) $(52)_{10} = (\quad)_2$ (2) $(101001011)_2 = (\quad)_{10}$ (3) $(11101110)_2 = (\quad)_8$ (4) $(68)_{10} = (\quad)_{16}$	**07**
20.	Define: Digital System**(March'10) [IMP]** Convert following Hexadecimal Number to Decimal B28, FFF, F28 Convert following Octal Number to Hexadecimal and Binary 414, 574, 725.25	**07**
21.	Convert the following numbers to decimal**(Dec'9) [IMP]** (i) $(1001.101)_2$ (ii) $(101011.11101)_2$ (iii) $(0.365)_8$ (iv) A3E5 (v) CDA4 (vi) $(11101.001)_2$ (vii) B2D4	**07**
22.	Perform the operation of subtractions with the following binary number using 2's complement**(Dec'9) [IMP]** (i) 10010 – 10011 (ii) 100 – 110000 (iii) 11010 – 10000	**07**
	1 (B) LOGIC CIRCUITS	
23.	Do as directed**(May'15 NEW) [IMP]** (v) Find the logic required at R input. 	**01**
24.	Discuss NAND gate as universal gate (implement NOT, AND OR & NOR gate using NAND gate).**(May'15 NEW) [IMP]**	**04**
25.	Define followings with respect to logic families.**(May'15 NEW) [IMP]/** (i) Fan in (ii) Fan out (iii) Noise Margin	**04**

	(iv) Propagation delay	
26.	Define and explain (i) fan out (ii) power dissipation and (iii) Propagation delay**(May'15) [IMP]/**	**07**
27.	Define the followings.**(Dec'14 NEW) [IMP]/** (i) Propagation delay (ii) Fan in (iii) Noise Margin (iii) Negative Logic	**04**
28.	Explain the digital IC Parameters.**(Dec'14) [IMP]/** 1. Fan in, Fan out 2. Propagation Delay 3. Power Dissipation 4. Noise Margin	**07**
29.	Explain briefly: propagation delay, fan out**(Dec'11) [IMP]/**	
30.	Answer the following**(May'11) [IMP]** (i) Define: Noise margin, Propagation delay	**02** **02**
31.	Draw and explain two input (i) AND (ii) OR and (iii) EX-OR gates.**(May'15) [IMP]**	**07**
32.	Select the most appropriate option**(Dec'14 NEW) [IMP]** (i) If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a high output? (A) 1 (B) 2 (C) 7 (D) 8 (ii) If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n): (A) AND (B) NAND (C) NOR (D) OR (iii) When used with an IC, what does the term "QUAD" indicate? (A) 2 circuits (B) 4 circuits (C) 6 circuits (D) 8 circuits	**03**
33.	Answer the following questions**(Dec'14) [IMP]/** 1. Find out Y, if B=1 and A=Square wave  2. explain SSI, MSI, LSI and VLSI	**05** **07**
34.	Define: Integrated Circuit and briefly explain SSI, MSI, LSI and VLSI**(March'10) [IMP]**	
35.	1. Give comparison for TTL and CMOS family. **(Dec'14) [IMP]** 2. Implement basic gates using DTL logic.	**07**
36.	Define the following terms:**(Nov'13) [IMP]** (1) Universal gate	**01**
37.	(1) Draw the logic circuit for following using only NAND gates:**(Nov'13) [IMP]** F = ABC+A'B+AC'D' (2) Draw the logic circuit for following using only NOR gates: F = ABC' + AB(C+D)	**07**
38.	Implement the Boolean functions. (a) xyz+x'y+xyz' (b) (A+B)'(A'+B')' and (c) F= xy+xy'+y'z with logic gates.**(May'13) [IMP]**	**07**
39.	Given Boolean function**(May'12) [IMP]** F = xy + x'y' + y'z 1. Implement it with only OR & NOT gates 2. Implement it with only AND & NOT gates	**05**
40.	Draw symbol and truth table for four input EX-OR gate. Explain NAND and NOR as an	**06**

	universal gate.**(Dec'11) [IMP]**	
41.	Explain NAND and NOR as an universal gates.**(May'11) [IMP]/**	**04**
42.	Explain with figures how NAND gate and NOR gate can be used as Universal gate.**(Dec'10) [IMP]**	**07**
43.	Implement Boolean expression for Ex-OR gate using NAND gates only**(May'11) [IMP]**	**04**
44.	Answer the following**(May'11) [IMP]** (i) Draw symbol and construct the truth table for three input Ex-OR gate.	**02**
45.	Draw the logic symbol and construct the truth table for each of the following gates. **(March'10) [IMP]** [1] Two input NAND gate [2] Three input OR gate [3] Three input EX-NOR gate [4] NOT gate	**07**
46.	Give classification of Logic Families and compare CMOS and TTL families **(March'10) [IMP]**	**07**
47.	Implement the following Boolean functions**(Dec'9) [IMP]** (i) F= A (B +CD) +BC' with NOR gates (ii) F= (A + B') (CD + E) with NAND gates	**07**
	2. BOOLEAN ALGEBRA AND MAPPING METHOD	
	2 (C) BOOLEAN ALGEBRA	
48.	State De-Morgan's theorems and prove with the help of truth table.**(May'15 NEW) [IMP]/**	**04**
49.	Define the followings.**(Dec'14 NEW) [IMP]/** (i) Write D'Morgan's Theorems	**01**
50.	State and prove demorgan's theorem**(Dec'14) [IMP]/**	**04**
51.	State and prove De-Morgan's Theorems with the help of Truth tables.**(Nov'13) [IMP]/**	**07**
52.	Demonstrate by means of truth tables the validity of the following Theorems of Boolean algebra**(Dec'9) [IMP]** (i) De Morgan's theorems for three variables	**3.5**
53.	Prove the following Boolean identities.**(Dec'14 NEW) [IMP]** (i) XY + YZ + Y' Z = XY + Z (ii) A . B + A' . B + A' . B' = A' + B	**07**
54.	Simplify using Boolean laws and draw the logic diagram for the given expression.**(Dec'14 NEW) [IMP]** F = (ABC)' + (AB)' C + A' B C' + A (BC)' + A B' C	**07**
55.	Simplify 1. A'B + A'BC' + A'BCD + A'BC'D'E**(Dec'14) [IMP]/(May'14) [IMP]** 2. (P+Q+R) (P'+ Q'+ R') P	**07/ 08**
56.	Prove that: 1. ((A'B+ABC)' + A(B+AB'))' = 0**(May'14) [IMP]** 2. AB'C + A'BC + ABC = AC + AB	**07**
57.	Simplify the following Boolean function to minimum numbers of literals.**(May'13) [IMP]** (a) xyz+x'y+xyz' and (b) (A+B)'(A'+B')'	**07**
58.	Obtain the truth table of the function F=xy+xy'+y'z OR Implement the Boolean functions.**(May'13) [IMP]**	**07**
59.	Show that the dual of the exclusive-OR is equal to its compliment.**(May'13) [IMP]**	**07**
60.	Find the complement of the following Boolean function and reduce to a minimum number of	**07**

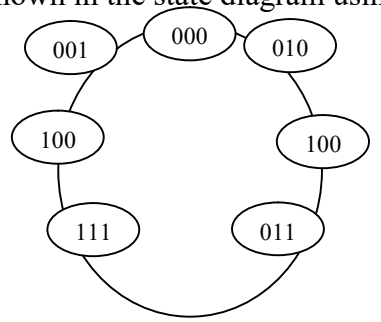
	literals.**(Dec'12) [IMP]** B'D + A'BC' + ACD + A'BC	
61.	Answer the following**(May'11) [IMP]** (i) What is the principle of Duality Theorem?	**02**
62.	Reduce the expression:**(Dec'10) [IMP]** (1) A+B(AC+(B+C')D) (2) (A+(BC)')'(AB'+ABC)	**07**
63.	Demonstrate by means of truth tables the validity of the following Theorems of Boolean algebra**(Dec'9) [IMP]** (ii) The Distributive law of + over .	**3.5**
	2 (D) MAPPING METHOD	
64.	Reduce the given function using K-map and implement the same using gates.**(May'15 NEW) [IMP]** F(A,B,C,D) = Σm (0,1,3,7,11,15) + Σd (2,4)	**07**
65.	Convert F(A, B, C) = BC + A into standard minterm form.**(May'15 NEW) [IMP]**	**03**
66.	Draw the truth table of full adder and implement using minimum number of logic gates.**(May'15 NEW) [IMP]/**	**07**
67.	Design a combinational circuits for a full adder.**(May'12) [IMP]/**	**04**
68.	Design a full-adder using two half-adder and an OR gate**(May'11) [IMP]/**	**07**
69.	With necessary sketch explain full adder in detail.**(Dec'9) [IMP]**	**07**
70.	Draw the truth table of full subtractor and implement using minimum number of logic gates.**(May'15 NEW) [IMP]**	**07**
71.	Express the Boolean function F=A+B'C a sum of minterms and in sum of max terms.**(May'15) [IMP]**	**07**
72.	Simplify the Boolean function $F_{(X,Y,Z)}= \sum(2,4,5,6)$ using K – map. Explain groups. **(May'15) [IMP]**	**07**
73.	Explain wired logic with examples.**(May'15) [IMP]**	**07**
74.	Design half adders and explain various implementations.**(May'15) [IMP]**	**07**
75.	Explain design and functioning of half and full subtractors.**(May'15) [IMP]**	**07**
76.	Design converter to convert decimal 8,4,-2,-1 code to BCD.**(May'15) [IMP]**	**07**
77.	Design converter to convert decimal 2,4,2,1 code to 8,4,-2,-1 code.**(May'15) [IMP]**	**07**
78.	Design BCD to excess – 3 code converter.**(May'15) [IMP] /**	**07**
79.	Design a BCD to Excess-3 code converter using minimum number of NAND gates**(Dec'14 NEW) [IMP]/ (Dec'11) [IMP]/**	**07/ 08**
80.	Design and implement BCD to excess 3 code converter.**(May'13) [IMP]**	**07**
81.	Minimize the following logic function using K-maps and realize using NAND and NOR gates.**(Dec'14 NEW) [IMP]** F(A,B,C,D) =Σ_m(1,3,5,8,9,11,15) + d(2,13).	**07**
82.	Minimize the logic function F (A,B,C,D) = π M (1, 2, 3, 8, 9, 10, 11, 14) . d (7, 15) Use Karnaugh map. Draw the logic circuit for simplified function using NOR gates only.**(Dec'14 NEW) [IMP]**	**07**
83.	A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations**(Dec'14 NEW) [IMP]**	**07**

	A is False, B is True A is False, C is True A, B, C are False A, B, C are True (i) Write the Truth table for F. Use the convention True = 1 and False = 0. (ii) Write the simplified expression for F in SOP form. (iii) Write the simplified expression for F in POS form. (iv) Draw the logic circuit using minimum number of 2-input NAND gates.	
84.	Reduce using K-map**(Dec'14) [IMP]** Σ m (0, 2, 6, 10, 11, 12, 13) + d (4, 5, 14, 15)	**07**
85.	Obtain the set of prime implicants for Σ m (0, 1, 6, 7, 8, 9, 13, 14, 15) **(Dec'14) [IMP]**	**07**
86.	Obtain the set of prime implicants for π M (2, 3, 8, 12, 13) . d (10, 14) **(Dec'14) [IMP]**	**07**
87.	Design a combinational circuit that multiplies BCD inputs by 5. Show that output can be obtained from the inputs without using any logic gates.**(Dec'14) [IMP]**	**07**
88.	Using K-map find the Boolean function and its complement for the following**(May'14) [IMP]** $F(A,B,C,D) = \sum(1,2,3,4,6,8,9,10,11,12,14)$	**07**
89.	Derive Boolean function using Tabulation Method for the following **(May'14) [IMP]** $F(P,Q,R,S) = \sum(0,1,3,4,5,7,10,13,14,15)$	**07**
90.	Attempt following:**(May'14) [IMP]** 1. Convert into Sum-of-Minterms: A' + B + CA 2. Convert into Product-of-Maxterms: A(A'+B)(C')	**07**
91.	Define the following terms:**(Nov'13) [IMP]** (1) Literal (2) Minterm (3) Maxterm	**03**
92.	Simplify the Boolean Function with Karnaugh map:**(Nov'13) [IMP]/** $F(_{W,X,Y,Z}) = \sum(0,1,2,4,5,6,8,9,12,13,14)$ and F = A'B'C' + B'CD' +A'BCD' +AB'C'	**07**
93.	Simplify the Boolean function:**(Dec'10) [IMP]/** (1) $F(w,x,y,z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$ (2) $F(w,x,y) = \sum(0,1,3,4,5,7)$	
94.	Simplify the Boolean function:**(Dec'10) [IMP]/** (1) F = A'B'C'+B'CD'+A'BCD'+AB'C' (2) F =A'B'D'+A'CD+A'BC d=A'BC'D+ACD+AB'D' Where "d" indicate Don't care conditions.	
95.	Simplify the following Boolean function using K-Map.**(May'12) [IMP]** F = A'B'C'+B'CD'+A'BCD'+AB'C'	**04**
96.	Simply the Boolean Function:**(Nov'13) [IMP]/** $F(_{W,X,Y,Z}) = \sum(1,3,7,11,15)$ and the Don't care conditions : $d(_{W,X,Y,Z}) = \sum(0,2,5)$	**07**
97.	Implement the functions $F=\sum(1,3,7,11,15)$ with don't care conditions $d= \sum(0,2,5)$ Discuss the effect of don't care conditions.**(May'13) [IMP]/**	**07**
98.	Simplify the Boolean Function using K-map**(May'11) [IMP]** $F(_{W,X,Y,Z}) = \sum(1, 3, 7, 11, 15)$ with don't care conditions $d(_{W,X,Y,Z}) = \sum(0, 2, 5)$	**04**
99.	Simplify the Boolean Function by using tabulation method:**(Nov'13) [IMP]/ (Dec'11) [IMP]/** $F = \sum(0,1,2,8,10,11,14,15)$	**07**

100. Simplify the following Boolean function using tabulation Method and draw logic diagram using NOR gates only**(May'11) [IMP]** $F(w,x,y,z) = \sum(0, 1, 2, 8, 10, 11, 14, 15)$	
101. With logic circuit describe the function of :**(Nov'13) [IMP]** (1) Full adder (2) Full subtractor Write the simplified Boolean functions with their outputs.	**07**
102. Define: combinational logic circuit**(Nov'13) [IMP]**	**01**
103. Obtain the simplified expression in sum of product for the following Boolean functions. **(May'13) [IMP]** (a) $F= \sum(0,1,4,5,10,11,12,14)$ and (b) $F= \sum(11,12,13,14,15)$.	**07**
104. Explain half and full adder in detail.**(May'13) [IMP]**	**07**
105. Show how a full-adder can be converted to a full-subtractor with the help of addition of one inverter circuit.**(Dec'12) [IMP]**	**07**
106. Obtain the simplified expressions in sum of products using K-map: x'z + w'xy' + w(x'y+xy')**(Dec'12) [IMP]**	**07**
107. Simplify the following Boolean function by means of the tabulation method:**(Dec'12) [IMP]/** $F(A,B,C,D,E,F,G) = (20,28,38,39,52,60,102,103,127)$ **108.** Determine the Prime Implicants of following Boolean Function using Tabulation Method.**(May'12) [IMP]** $F(A,B,C,D,E,F,G) = \sum(20,28,38,39,52,60,102,103,127)$	**07**
109. Design a combinational circuit with the four input lines that represent a decimal digit in BCD and four output line that generate the 9's complement of the input digit.**(Dec'12) [IMP]/** **110.** Design a combinational circuit that generates the 9's complement of BCD digit.**(Dec'9) [IMP]**	**07** **07**
111. Design the Combinational Circuits for Binary to Gray Code Conversion.**(May'12) [IMP]**	**05**
112. Explain Design Procedure for Combinational Circuit & Difference between Combinational Circuit & Sequential Circuit.**(May'12) [IMP]**	**04**
113. Express following Function in Product of Maxterms**(May'12) [IMP]** $F(x,y,z)=(xy + z) (y + xz)$	**03**
114. Explain briefly: SOP & POS, minterm & maxterm, canonical form**(Dec'11) [IMP]**	**03**
115. Simplify Boolean function $F (w,x,y,z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$ using K-map and Implement it using (i) NAND gates only (ii) NOR gates only**(Dec'11) [IMP]**	**08**
116. Design a combinational circuit whose input is a four bit number and whose Output is the 2's complement of the input number.**(Dec'11) [IMP]/ (May'11) [IMP]**	**08/ 07**
117. Answer the following**(May'11) [IMP]** (i) Explain briefly: standard SOP and POS forms. (ii) What are Minterms and Maxterms?	**04**
118. Explain SOP and POS expression using suitable examples**(March'10) [IMP]**	**07**
119. Design 4 bit binary to BCD code converter**(March'10) [IMP]**	**07**
120. Obtain the simplified expressions in sum of products for the following Boolean functions:**(Dec'9) [IMP]** (i) $F(A,B,C,D,E) = \sum(0,1,4,5,16,17,21,25,29)$ (ii) A'B'CE' + A'BCD' + B'DE' + BCD'	**07**

121. Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number.**(Dec'9) [IMP]**	**07**
3. LOGIC FUNCTION REALIZATION WITH MSI CIRCUITS	
122. Design a circuit for 2-bit magnitude comparator.**(May'15 NEW) [IMP]**	**07**
123. Design 3-bit even parity generator circuit.**(May'15 NEW) [IMP]**	**07**
124. Design 4 X 16 decoder using two 3 X 8 decoder.**(May'15 NEW) [IMP]/ (Dec'12) [IMP]/** **125.** Design a 4-to-16 decoder by using only 2-4 decoder circuits.**(May'14) [IMP]/** **126.** Construct 4*16 Decoder with help of 2*4 Decoder.**(May'12) [IMP]**	**07** **05**
127. Implement the given function using 8 X 1 Multiplexer.**(May'15 NEW) [IMP]** $F(A,B,C,D) = \sum m(0,1,2,3,5,8,9,11,14)$	**07**
128. Design a BCD adder.**(May'15) [IMP]/** **129.** Discuss 4 bit BCD adder in detail.**(May'12) [IMP]**	**07** **05**
130. Explain 3 to 8 line decoder.**(May'15) [IMP]/** **131.** With logic circuit and truth table explain working of 3 to 8 line decoder.**(Nov'13) [IMP] /(Dec'10) [IMP]** **132.** What is meant by decoder? Explain 3-to-8 line decoder with diagram and truth table **(Dec'11) [IMP]/**	**07**
133. Design a 8 to 1 multiplexer by using the four variable function given by **(Dec'14 NEW) [IMP]** $F(A,B,C,D) = \sum m(0,1,3,4,8,9,15)$	**07**
134. Implement F (A, B, C, D) = Σ m (0, 1, 3, 4, 8, 9, 15) using multiplexer, choose A as input line.**(Dec'14) [IMP]/** **135.** What is multiplexer? Implement the following function with a multiplexer $F(A,B,C,D) = \sum(0, 1, 3, 4, 8, 9, 15)$**(May'11) [IMP]**	**07**
136. Design a combinational circuit that accepts the decimal number in BCD and display it on seven segment display.**(Dec'14) [IMP]**	**07**
137. Write a brief note on parity checker/generator.**(May'14) [IMP]**	**07`**
138. What is encoder? With logic circuit and truth table explain the working of Octal to binary Encoder.**(Nov'13) [IMP]**	**07**
139. What is Multiplexer? With logic circuit and function table explain the working of 4 to 1 multiplexer.**(Nov'13) [IMP]** / **140.** Explain a 4 to 1 line multiplexer in detail.**(May'13) [IMP] /** **141.** What is meant by multiplexer? Explain with diagram and truth table the Operation of 4-to-1 line multiplexer**(Dec'11) [IMP]/** **142.** With logic diagram and function table explain the operation of 4 to 1 line multiplexer.**(Dec'10) [IMP]**	**07**
143. With logic circuit explain the working of 4-bit magnitude comparator.**(Nov'13) [IMP]/** **144.** Explain 4 bit Magnitude Comparator.**(May'12) [IMP]/ (Dec'9) [IMP]**	**07**
145. Explain common cathode types seven segments displays. **(May'12) [IMP]**	**03**
146. Design a BCD to decimal decoder **(May'11) [IMP]**	**07**
147. A combinational circuit is defined by functions:**(May'11) [IMP]** $F1(A,B,C) = \sum(3, 5, 6, 7)$	

	F2(A,B,C) = ∑(0, 2, 4, 7) Implement the circuit with PLA having three inputs, four product term and two outputs	
148.	Design a full adder circuit using decoder and multiplexer**(March'10) [IMP]**	**07**
149.	Define: [1] Comparator [2] Encoder [3] Decoder [4] Multiplexer [5] De-multiplexer **(March'10) [IMP]**	**05**
	4. FLIP-FLOPS, COUNTERS AND REGISTERS	
	4 (C) FLIP-FLOPS	
150.	Convert D flip flop into SR flip flop.**(May'15 NEW) [IMP]**	**07**
151.	With the help of function table and circuit diagram explain the working of clocked SR flip flop.**(May'15 NEW) [IMP]/**	**07**
152.	1. Convert J K Flip Flop to S R Flip flop.**(Dec'14) [IMP]/** 2. Show the logical diagram of clocked S R Flip flop with AND and NOR gates.	**07**
153.	With neat sketch explain the operation of clocked RS flip-flop**(Dec'9) [IMP]**	**05**
154.	Draw the circuit diagrams and Truth table of all the Flip flops (SR, D, T and JK). **(Dec'14 NEW) [IMP]**	**07**
155.	Implement D flip flop using JK flip flop.**(Dec'14 NEW) [IMP]**	**07**
156.	Draw and explain Master – slave Flip flop.**(Dec'14) [IMP]/**	**07**
157.	Write a note on Master-Slave Flip-Flop.**(May'14) [IMP]/**	
158.	With logic diagram explain the function of master-slave flip-flop.**(Nov'13) [IMP]/**	**05**
159.	Explain Master Slave Flip Flop through J K Flip Flop.**(May'12) [IMP]**	**04**
160.	Explain the working of the Master Slave J K flip-flop**(Dec'11) [IMP]/**	**06**
161.	Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram**(May'11) [IMP]**	**07**
162.	Write a brief note on edge-triggered SR and JK Flip-Flops.**(May'14) [IMP]**	**07**
163.	Design a sequential circuit using JK Flip-Flops and two states Q0 and Q1 such that, 1. It moves to the next state for input 0. (00 to 01, 01 to 10,…, 11 to 00) 2. It moves to the previous state for input 1. (reverse from the above mentioned steps) **(May'14) [IMP]**	**09**
164.	Define the following terms:**(Nov'13) [IMP]** (1) Flip Flop	**01**
165.	Define: sequential logic circuit**(Nov'13) [IMP]**	**01**
166.	Design a sequential with JK flip-flops to satisfy the following state equations:**(Nov'13) [IMP]/(May'12) [IMP]** A(t+1) = A'B'CD+A'B'C+ACD+AC'D' B(t+1) = A'C+CD'+A'BC' C(t+1) = B D(t+1) = D'	**07**
167.	Explain D type positive edge triggered flip flop.**(May'13) [IMP]/**	**07**
168.	Discuss D-type edge- triggered flip-flop in detail.**(Dec'9) [IMP]**	
169.	Explain JK Flipflop. What is disadvantage of it and how it can be eliminated?**(Dec'12) [IMP]**	**07**
170.	Explain the procedure followed to analyse a clocked sequential circuit With suitable	**10**

example**(Dec'11) [IMP]**	
171. Define: state table, state equation, state diagram, input & output equations**(Dec'11) [IMP]**	**04**
172. Answer the following**(May'11) [IMP]** (i) Give comparison between combinational and Sequential circuits (ii) What is race-around condition in JK flip-flop?	**04**
173. Draw logic diagram, graphic symbol, and Characteristic table for clocked D flip-flop**(May'11) [IMP]/**	**03**
174. Show the logic diagram of clocked D**(Dec'9) [IMP]**	**02**
175. With logic diagram and truth table explain the working JK Flipflop. Also obtain its characteristic equation. How JK flip-flop is refinement of RS flip-flop?**(Dec'10) [IMP]**	**07**
176. Define: [1] Flip-Flop**(March'10) [IMP]**	**01**
177. Draw and explain working of following flip-flops.**(March'10) [IMP]** [1] Clocked RS [2] JK	**07**
178. Convert SR flip-flop into JK flip-flop**(March'10) [IMP]**	**07**
179. Design sequential counter as shown in the state diagram using JK flip-flops. **(March'10) [IMP]**  Clockwise direction to follow	**07**
4 (F) COUNTERS	
180. Design 4-bit ripple counter using negative edge triggered JK flip flop.**(May'15 NEW) [IMP]/** **181.** Write a note on Binary Ripple Counter.**(May'14) [IMP]/** **182.** With logic diagram explain the operation of 4 bit binary ripple counter. How up counter can be converted into down counter?**(Nov'13) [IMP] /(Dec'10) [IMP]/** **183.** Explain 4 bit binary ripple counter.**(May'12) [IMP]/** **184.** Explain working of 4-bit binary ripple counter**(Dec'11) [IMP]** **185.** Give classification of counters and explain asynchronous 4-bit binary ripple counter**(May'11) [IMP]** **186.** Explain the working of 4 bit asynchronous counter**(March'10) [IMP]**	**07**
187. Design a mod-12 Synchronous up counter using D-flip flop.**(Dec'14 NEW) [IMP]**	**07**
188. Design a synchronous BCD counter with JK Flip flop.**(Dec'14) [IMP] /** **189.** Design a synchronous BCD counter with JK Flip flops.**(May'13) [IMP]**	**07**
190. Design and explain 4-bit Ripple UP/DOWN Counter using positive edge triggered Flip flop.**(Dec'14) [IMP]**	**07**
191. Design and implement a Modulo-6 Asynchronous counter using T Flip flop.**(Dec'14) [IMP]**	**07**
192. Design and Implement a Mod-10 asynchronous counter with T FF.**(May'14) [IMP]**	**07**
193. Define the following terms:**(Nov'13) [IMP]** (1) Counter	**01**

194. Design a counter with the following binary sequence:**(Dec'12) [IMP]/ (Dec'9) [IMP]** 0, 1, 3, 7, 6, 4 and repeat. Use T flipflop.	**07**
195. Explain BCD Ripple counter and draw its logic diagram and timing diagram.**(Dec'12) [IMP]/** **196.** Draw the state diagram of BCD ripple counter, develop it's logic diagram, and explain it's operation.**(Dec'9) [IMP]**	**07**
197. Explain 4-bit up-down binary synchronous counter.**(May'12) [IMP]**	**07**
198. Design counter with the following binary sequence:**(Dec'10) [IMP]/ (Dec'9) [IMP]** 0, 4,2,1,6 and repeat. Use JK flip-flops	**07**
4 (G) REGISTERS	
199. With neat sketch design 4-bit bidirectional shift register.**(May'15 NEW) [IMP]**	**07**
200. Write a short note on four bit Universal Shift Register.**(Dec'14 NEW) [IMP]/** **201.** Explain in detail bidirectional shit register with parallel load.**(Dec'12) [IMP] /** **202.** Draw and explain the block diagram of 4-bit bidirectional shit register with Parallel load. **(Dec'11) [IMP]/** **203.** With necessary sketch explain Bidirectional Shift Register with parallel load.**(Dec'9) [IMP]**	**07**
204. Design a circuit for 4-bits parallel register with load with D Flip-Flops. Load input decides whether to load new input or to apply no change conditions.**(May'14) [IMP]**	**07**
205. Define the following terms:**(Nov'13) [IMP]** (1) Register	**01**
206. What is the difference between serial and parallel transfer? What type of registers are used in each case.**(May'13) [IMP]**	**07**
207. Explain Johnson Counters.**(May'12) [IMP]/** **208.** Construct a Johnson counter with Ten timing signals.**(Dec'9) [IMP]**	**07**
209. Define the different mode of operation of registers & explain any two in details. **(May'12) [IMP]**	**07**
210. How many flip flops are required to build a shift register to store following numbers?**(May'12) [IMP]** i) Decimal 28 ii) Binary 6 bits iii) Octal 17 iv) Hexadecimals A	**04**
211. What is the function of shift register? With the help of simple diagram explain its working. With block diagram and timing diagram explain the serial transfer of information from register A to register B.**(Dec'10) [IMP]**	**07**
5. INTRODUCTION TO STATE MACHINES	
212. Define followings with respect to finite state machine.**(May'15 NEW) [IMP]** (i) State table (ii) Melay machine (iii) Moore machine	**03**
213. Discuss the General State machine Architecture.**(Dec'14 NEW) [IMP]**	**07**

6. SYNCHRONOUS STATE MACHINE DESIGN	
7. ASYNCHRONOUS STATE MACHINES	
214. Explain the Fundamental Mode Model of Asynchronous State Machine with suitable example.**(Dec'14 NEW) [IMP]**	**07**
8. LOGIC FAMILIES	
215. Select the most appropriate option**(Dec'14 NEW) [IMP]** (i) Which TTL logic gate is used for wired ANDing (A) Open collector output (B) Totem Pole (C) Tri state output (D) ECL gates	**01**
216. Define the followings.**(Dec'14 NEW) [IMP]** (i) Totem Pole output	**01**
217. Compare the following in every aspect.**(Dec'14 NEW) [IMP]** (i) TTL and CMOS	**3.5**
9. PROGRAMMABLE LOGIC DEVICES	
218. Compare ROM, PLA and PAL.**(May'15 NEW) [IMP]**	**07**
219. Explain ROM and it's types.**(May'15) [IMP]/** **220.** Write short note on: Read Only Memory (ROM)**(May'11) [IMP]/** **221.** Write short note on EEPROM, EPROM and PROM**(March'10) [IMP]**	**07**
222. Explain PLA and it's application.**(May'15) [IMP] /** **223.** Write short note on Programmable Logic Arrays.**(Dec'14 NEW) [IMP]/** **224.** Explain in brief: Programmable Logic Array**(May'14) [IMP]/** **225.** Explain PLA in detail.**(May'13) [IMP] /** **226.** Explain PLA with necessary diagrams.**(Dec'12) [IMP]**	**07**
227. Define the followings.**(Dec'14 NEW) [IMP]** (i) EPROM	**01**
228. Compare the following in every aspect.**(Dec'14 NEW) [IMP]** (i) RAM and ROM	**3.5**
229. A combinational circuit is defined by functions:**(May'11) [IMP]** $F1(A,B,C) = \sum(3, 5, 6, 7)$ $F2(A,B,C) = \sum(0, 2, 4, 7)$ Implement the circuit with PLA having three inputs, four product term and two outputs	**07**
230. Define: [1] PLA**(March'10) [IMP]**	**01**
231. Explain memory unit**(March'10) [IMP]**	**07**