AMIRAJ

COLLEGE OF ENGINEERING & TECHNOLOGY

LABORATORY MANUAL

ANALOG AND DIGITAL ELECTRONICS

SUBJECT CODE: 3130907

DEPARTMENT OF ELECTRICAL ENGINEERING

B.E. 3rd SEMESTER

NAME:_____
ENROLLMENT NO: _____
BATCH NO: _____
YEAR: _____

Amiraj College of Engineering and Technology,
Nr.Tata Nano Plant, Khoraj, Sanand, Ahmedabad.

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COLLEGE OF ENGINEERING & TECHNOLOGY

Amiraj College of Engineering and Technology,

Nr.Tata Nano Plant, Khoraj, Sanand, Ahmedabad.

CERTIFICATE

This is to certify that Mr. / Ms. _____

Of class_____ Enrolment No _____has

Satisfactorily completed the course in _____as

by the Gujarat Technological University for ____ Year (B.E.) semester___ of

Mechanical Engineering in the Academic year_____.

Date of Submission:-

Faculty Name and Signature

(Subject Teacher)

Head of Department

(ELECTRICAL)

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SUBJECT: ANALOG AND DIGITAL ELECTRONICS

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List Of Experiments

Sr. No.	Title	Date of Performance	Date of submission	Sign	Remark
1.	Darlington Amplifier				
2.	Differential Amplifiers- Transfer characteristic.				
3.	CMRR Measurement				
4.	Cascade amplifier				
5.	Determination of bandwidth of single stage and multistage amplifiers				
6.	Spice Simulation of Common Emitter and Common Source amplifiers				
7.	Design implementation of code Converter				
8.	Design and implementation of 4 bit binary Adder/Subtractor and BCD adder using IC 7483				
9.	Design and implementation of Multiplexer and De-multiplexer using logic gates				
10.	Design and implementation of encoder and decoder using logic gates				
11.	Design and implementation of 3-bit synchronous up/down counter				

EXPERIMENT NO 1: DARLINGTON AMPLIFIER USING BJT

AIM: Construct Darlington Amplifier using BJT.

Apparatus Required:

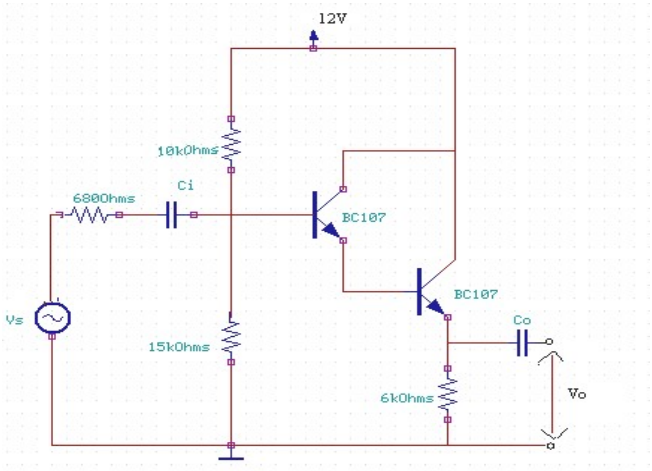
S.No.	Name	Range	Quantity
1.	Transistor	BC 107	1
2.	Resistor	15kΩ,10kΩ,680Ω,6kΩ	1,1,1,1
3.	Capacitor	0.1μF, 47μF	2, 1
4.	Function Generator	(0-3)MHz	1
5.	CRO	30MHz	1
6.	Regulated power supply	(0-30)V	1
7.	Bread Board		1

Theory:

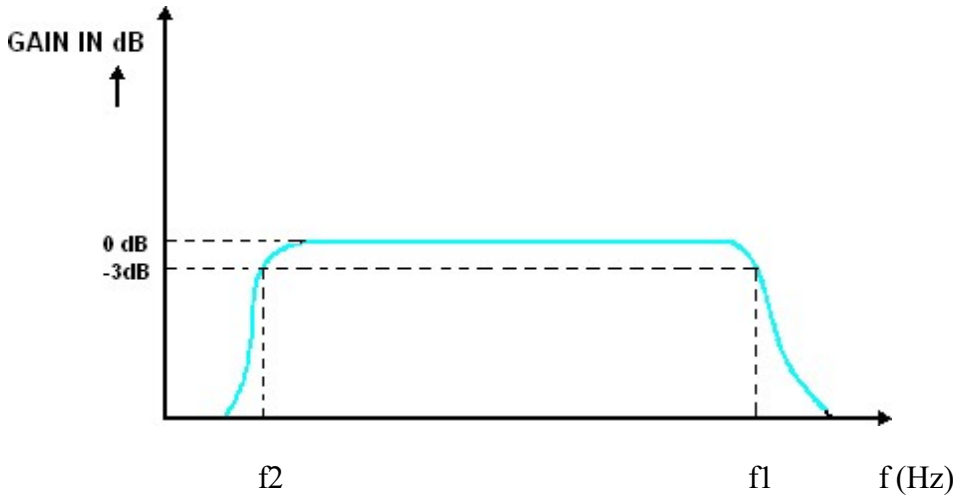
In Darlington connection of transistors, emitter of the first transistor is directly connected to the base of the second transistor .Because of direct coupling dc output current of the first stage is (1+h*fe*)Ib1.If Darlington connection for n transitor is considered, then due to direct coupling the dc output current foe last stage is (1+h*fe*) n times Ib1 .Due to very large amplification factor even two stage Darlington connection has large output current and output stage may have to be a power stage. As the power amplifiers are not used in the amplifier circuits it is not possible to use more than two transistors in the Darlington connection.

In Darlington transistor connection, the leakage current of the first transistor is amplified by the second transistor and overall leakage current may be high, which is not desired.

Circuit Diagram:



Model Graph:



Tabular Form:

Keep the input voltage constant, Vin =

Frequency (in Hz)	Output Voltage (in volts)	Gain= 20 log(Vo/Vin) (in dB)

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mv, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) vs Frequency(Hz).
5. Calculate the bandwidth from the graph.

Result:

Thus, the Darlington current amplifier was constructed and the frequency response curve is plotted. . The Gain Bandwidth Product is found to be =

EXPERIMENT NO 2: DIFFERENTIAL AMPLIFIER USING BJT

Aim:

To construct a differential amplifier using BJT and to determine the dc collector current of individual transistors.

Apparatus Required:

S.No.	Name	Range	Quantity
1.	Transistor	BC107	2
2.	Resistor	4.7kΩ, 10kΩ	2,1
3.	Regulated power supply	(0-30)V	1
4.	Function Generator	(0-3) MHz	2
5.	CRO	30 MHz	1
6.	Bread Board		1

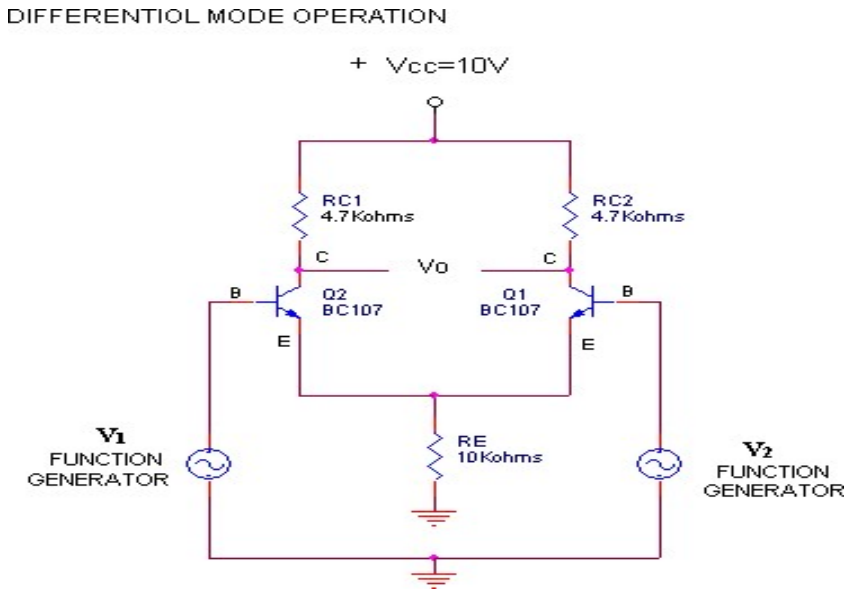
Theory:

The differential amplifier is a basic stage of an integrated operational amplifier. It is used to amplify the difference between 2 signals. It has excellent stability, high versatility and immunity to noise. In a practical differential amplifier, the output depends not only upon the difference of the 2 signals but also depends upon the common mode signal.

Transistor Q1 and Q2 have matched characteristics. The values of RC1 and RC2 are equal. Re1 and Re2 are also equal and this differential amplifier is called emitter coupled differential amplifier. The output is taken between the two output terminals.

For the differential mode operation the input is taken from two different sources and the common mode operation the applied signals are taken from the same source

Circuit Diagram:



Observation:

VIN =VO =AC = VO / VIN
VIN = V1 – V2
V0 =
Ad = V0/ VIN

Procedure:

1. Connections are given as per the circuit diagram.
2. To determine the common mode gain, we set input signal with voltage Vin=2V and determine Vo at the collector terminals. Calculate common mode gain, Ac=Vo/Vin.
3. To determine the differential mode gain, we set input signals with voltages V1 and V2. Compute Vin=V1-V2 and find Vo at the collector terminals. Calculate differential mode gain, Ad=Vo/Vin.
4. Calculate the CMRR=Ad/Ac.
5. Measure the dc collector current for the individual transistors.

Result:

Thus, the Differential amplifier was constructed and dc collector current for the individual transistors is determined.

EXPERIMENT NO 3: DIFFERENTIAL AMPLIFIER USING BJT

Aim:

To construct a differential amplifier using BJT and to calculate the CMRR.

Apparatus Required:

S.No.	Name	Range	Quantity
1.	Transistor	BC107	2
2.	Resistor	4.7kΩ, 10kΩ	2,1
3.	Regulated power supply	(0-30)V	1
4.	Function Generator	(0-3) MHz	2
5.	CRO	30 MHz	1
6.	Bread Board		1

Formula:

Common mode Gain (Ac) = VO / VIN

Differential mode Gain (Ad) = V0 / VIN

Where VIN = V1 – V2

Common Mode Rejection Ratio (CMRR) = Ad/Ac

Where, Ad is the differential mode gain

Ac is the common mode gain.

Theory:

The differential amplifier is a basic stage of an integrated operational amplifier. It is used to amplify the difference between 2 signals. It has excellent stability, high versatility and immunity to noise. In a practical differential amplifier, the output depends not only upon the difference of the 2 signals but also depends upon the common mode signal.

Transistor Q1 and Q2 have matched characteristics. The values of RC1 and RC2 are equal. Re1 and Re2 are also equal and this differential amplifier is called emitter coupled differential amplifier. The output is taken between the two output terminals.

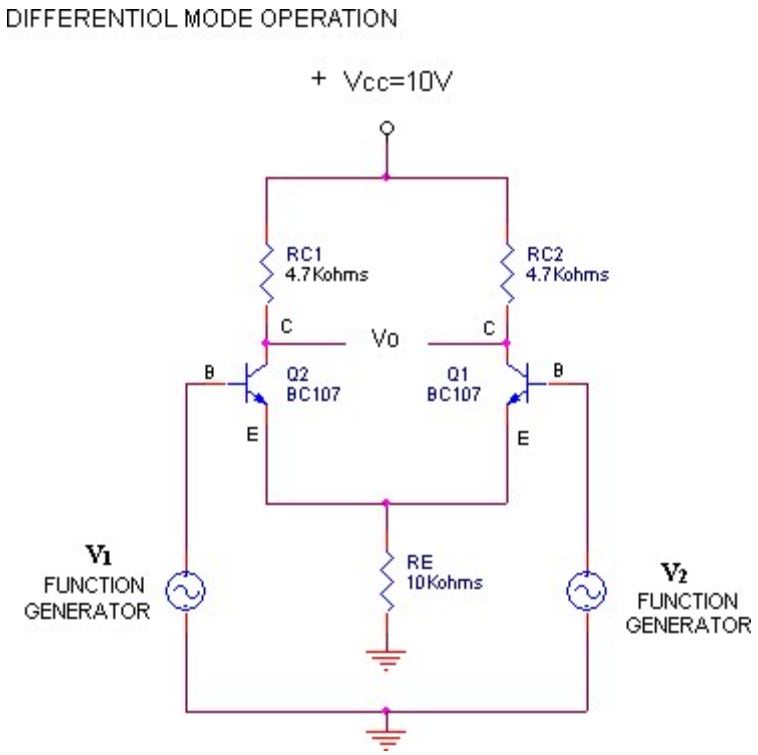
For the differential mode operation the input is taken from two different sources and the common mode operation the applied signals are taken from the same source

Common Mode Rejection Ratio (CMRR) is an important parameter of the differential amplifier. CMRR is defined as the ratio of the differential mode gain, Ad to the common mode gain, Ac.

$$CMRR = Ad / Ac$$

In ideal cases, the value of CMRR is very high.

Circuit Diagram:



Observation:

VIN =VO =AC = VO / VIN
VIN = V1 – V2
V0 =
Ad = V0/ VIN

Procedure:

1. Connections are given as per the circuit diagram.
2. To determine the common mode gain, we set input signal with voltage Vin=2V and determine Vo at the collector terminals. Calculate common mode gain, Ac=Vo/Vin.
3. To determine the differential mode gain, we set input signals with voltages V1 and V2. Compute Vin=V1-V2 and find Vo at the collector terminals. Calculate differential mode gain, Ad=Vo/Vin.
4. Calculate the CMRR=Ad/Ac.
5. Measure the dc collector current for the individual transistors.

Result:

Thus, the Differential amplifier was constructed and the CMRR is calculated.

EXPERIMENT NO 4: CASCADE AMPLIFIER

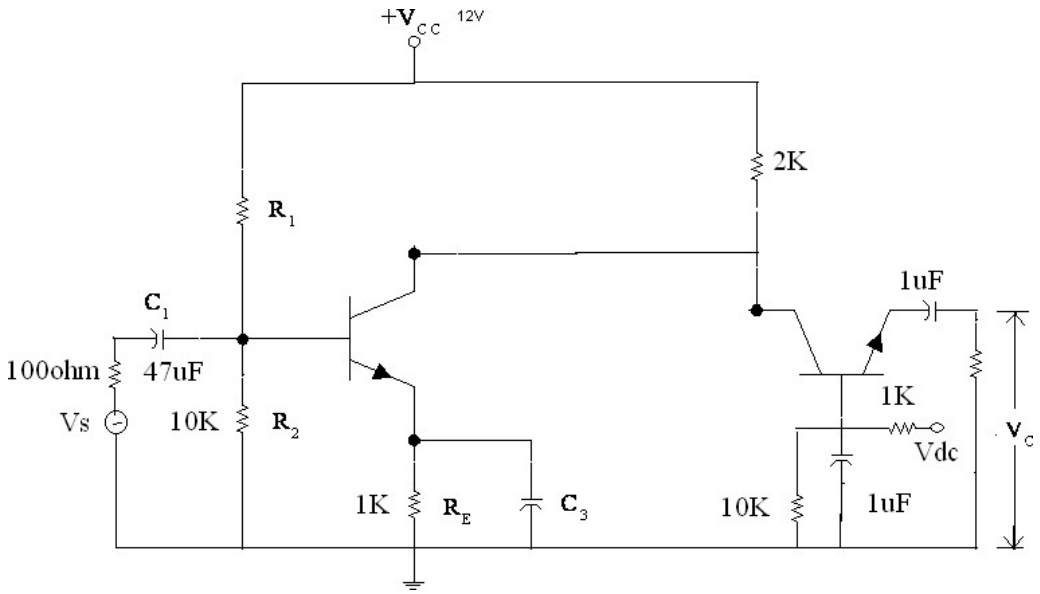
Aim:

To measure voltage gain, input resistance and output resistance of cascade Amplifier.

Apparatus:

S.No.	Name	Range	Quantity
1.	Transistor	BC107	2
2.	Resistor	1kΩ, 100Ω,10KΩ,2KΩ	2,1 ,1,2
3.	Capacitor	1μf,47μf	3,1
4.	Regulated power supply	(0-30)V	1
5.	Function Generator	(0-3) MHz	1
6.	CRO	30 MHz	1
7.	Bread Board		1

Circuit Diagram:



Theory:

Cascode amplifier is a cascade connection of a common emitter and common base amplifiers. It is used for amplifying the input signals. The common application of cascade amplifier is for impedance matching. The low impedance of CE age is matched with the medium of the CB sage.

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mV, using the signal generator
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Calculate the voltage gain, input resistance and output resistance of cascade Amplifier.

Design:

IB1=VCE-VBE/RB1
IC1=IE2=IC2=ßIB1
VC1=VE2=VB2-VBE
VC2=VCC-IC2*RC2
VCE2=VC2-VE2
Rin=RB1 ||ß1RE1
Av1=-RL1/RE1=-1
Ro=RC2
RL2=RC2 ||RL
AV2=RL2/RE2
Av=AV1*AV2

Result:

Thus, the voltage gain, input resistance and output resistance of cascade Amplifier was measured.

EXPERIMENT NO 5: DETERMINATION OF BANDWIDTH OF SINGLE STAGE AND MULTISTAGE AMPLIFIERS

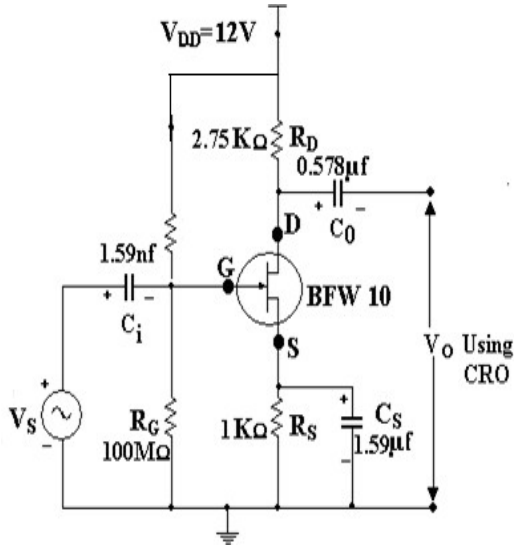
Aim:

To determine the bandwidth of Single Stage and Multistage Amplifiers.

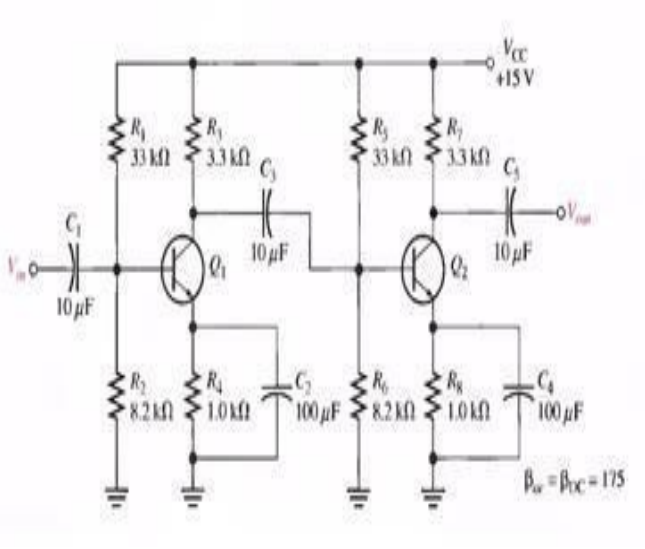
Apparatus:

S.No.	Name	Range	Quantity
1.	FET , Transistor	BFW10 , BC107	1,2
2.	Resistor	100MΩ, 1kΩ,2.75KΩ,33KΩ,10KΩ,8.2KΩ	1,1,2 ,4,2,2
3.	Capacitor	1.59nf, 0.578µf,10µf,100µf	2,1,3,2
4.	Regulated power supply	(0-30)V	1
5.	Function Generator	(0-3) MHz	2
6.	CRO	30 MHz	1
7.	Bread Board		1

Circuit Diagram:



Single Stage Common Source Amplifier



Multistage Amplifier

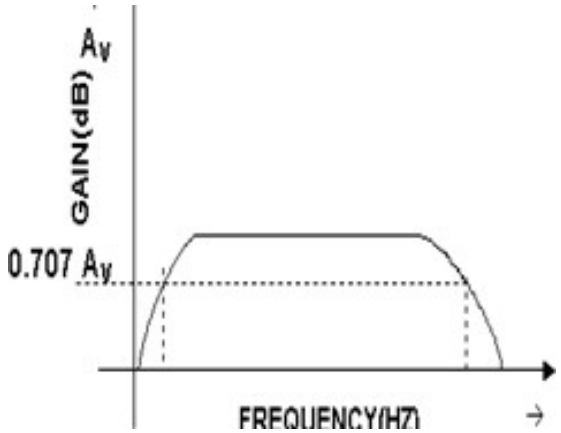
Theory:

The CS amplifier is a small signal amplifier. For good bias stability, the source resistor voltage drop should be as large as possible. Where the supply voltage is small, Vs may be reduced to a minimum to allow for the minimum level of Vds.R2 is usually selected as 1MΩ or less as for BJT capacitor coupled circuit, coupling and bypass capacitors should be selected to have the smallest possible capacitance values. The largest capacitor in the circuit sets the circuit low 3dB frequency (capacitor C2). Generally to have high input impedance FET is used. As in BJT circuit RL is usually much larger than Zo and Zi is often much larger than Rs.

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Give 1 KHz signal and 25 mv (P-P) as Vs from signal generator.
3. Observe the output on CRO for proper working of the amplifier.
4. After ensuring the amplifier function, vary signal frequency from 50 Hz to 600 Hz in proper steps for 15-20 readings keeping Vs =25mv(PP) at every frequency ,note down the resulting output voltage and tabulate it.

Model Graph:



Result:

Thus, the bandwidth of Single Stage and Multistage Amplifier was determined.

EXPERIMENT NO 6: SPICE SIMULATION OF COMMON EMITTER AND COMMON SOURCE AMPLIFIERS

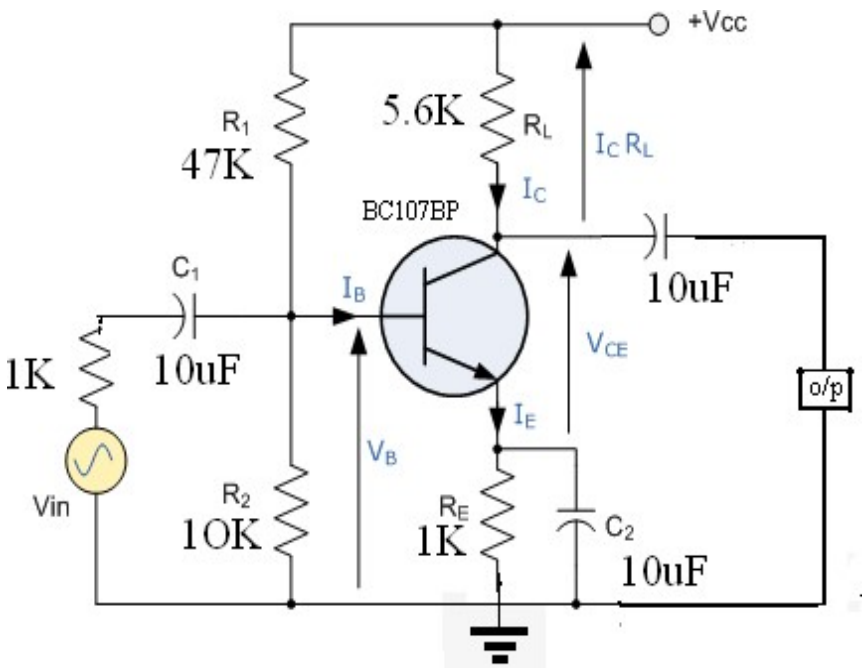
Aim:

To Simulate the Common Emitter and Common Source Amplifiers using SPICE software.

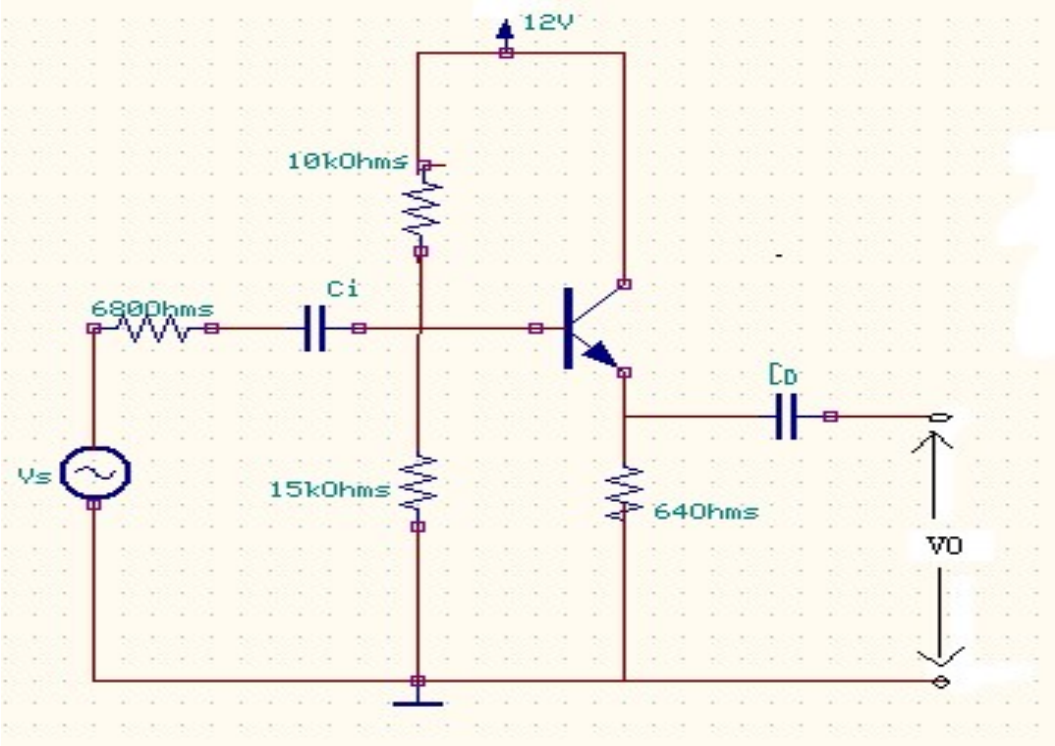
Apparatus:

S.No.	Name	Range	Quantity
1.	Transistor	BC710	1
2.	Resistor	47KΩ,5.6KΩ,10KΩ,1 KΩ,680Ω,640Ω,15KΩ	1,1,2,1,1,1 ,1
3.	Capacitor	10µf	3
4.	Regulated power supply	(0-30)V	1
5.	Function Generator	(0-3) MHz	1
6.	CRO	30 MHz	1
7.	Bread Board		1

Circuit Diagram:



Common Emitter Amplifiers



Common Source Amplifiers

Theory:

Common Emitter Amplifiers

The CE amplifier is a small signal amplifier. This small signal amplifier accepts low voltage ac inputs and produces amplified outputs. A single stage BJT circuit may be employed as a small signal amplifier; has two cascaded stages give much more amplification. Designing for a particular voltage gain requires the use of a ac negative feedback to stabilize the gain. For good bias stability, the emitter resistor voltage drop should be much larger than the base -emitter voltage. And Re resistor will provide the required negative feedback to the circuit. CE is provided to provide necessary gain to the circuit. All bypass capacitors should be selected to have the smallest possible capacitance value, both to minimize the physical size of the circuit for economy. The coupling capacitors should have a negligible effect on the frequency response of the circuit.

Common Source Amplifiers

The D.C biasing in common collector is provided by R1, R2 and RE .The load resistance is capacitor coupled to the emitter terminal of the transistor.

When a signal is applied to the base of the transistor, VB is increased and decreased as the signal goes positive and negative, respectively. Considering VBE is constant the variation in the VB appears at the emitter and emitter voltage VE will vary same as base voltage VB . Since the emitter is output terminal, it can be noted that the output voltage from a common collector circuit is the same as its input voltage. Hence the common collector circuit is also known as an emitter follower.

Procedure for Common Emitter Amplifiers:

1. Connect the circuit as per the circuit diagram.
2. Give l00Hz signal and 20mv p-p as Vs from the signal generator
3. Observe the output on CRO and note down the output voltage.
4. Keeping input voltage constant and by varying the frequency in steps 100Hz-1MHz, note down the corresponding output voltages.
5. Calculate gain in dB and plot the frequency response on semi log sheet

Procedure for Common Source Amplifiers:

1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mV, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) Vs Frequency (Hz).

Result:

Thus, the Common Emitter and Common Source Amplifiers are simulated using SPICE software.

EXPERIMENT NO 7: DESIGN AND IMPLEMENTATION OF CODE CONVERTOR

Aim:

To design and implement 4-bit

(i) Binary to gray code converter
(ii) Gray to binary code converter
(iii) BCD to excess-3 code converter
(iv) Excess-3 to BCD code converter

APPARATUS REQUIRED:

Sl.No.	Component	Specification	Qty.
1.	X-OR GATE	IC 7486	1
2.	AND GATE	IC 7408	1
3.	OR GATE	IC 7432	1
4.	NOT GATE	IC 7404	1
5.	IC TRAINER KIT	-	1
6.	PATCH CORDS	-	35

THEORY:

The availability of large variety of codes for the same discrete elements of information results in the use of different codes by different systems. A conversion circuit must be inserted between the two systems if each uses different codes for same information. Thus, code converter is a circuit that makes the two systems compatible even though each uses different binary code.

The bit combination assigned to binary code to gray code. Since each code uses four bits to represent a decimal digit. There are four inputs and four outputs. Gray code is a non-weighted code.

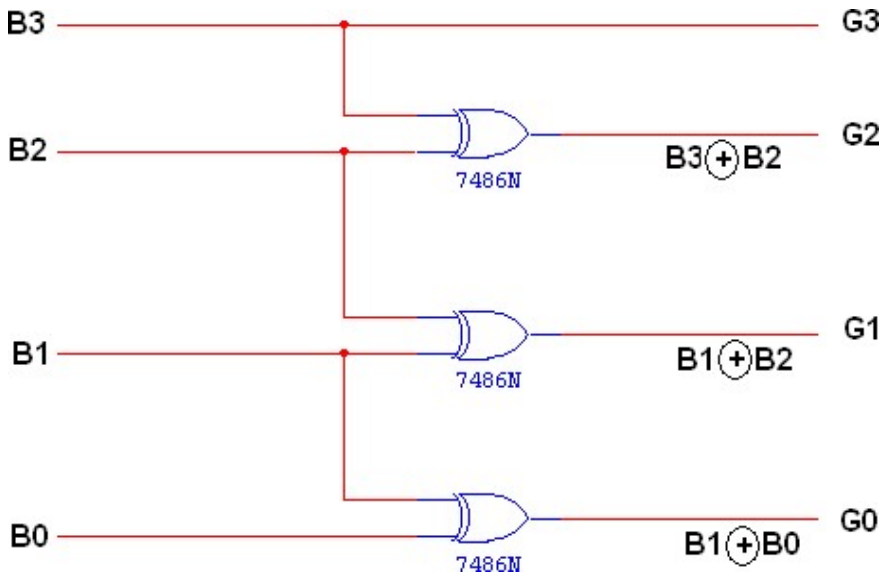
The input variable are designated as B3, B2, B1, B0 and the output variables are designated as C3, C2, C1, Co. from the truth table, combinational circuit is designed. The Boolean functions are obtained from K-Map for each output variable.

A code converter is a circuit that makes the two systems compatible even though each uses a different binary code. To convert from binary code to Excess-3 code, the input lines must supply the bit combination of elements as specified by code and the output lines generate the corresponding bit combination of code. Each one of the four maps represents one of the four outputs of the circuit as a function of the four input variables.

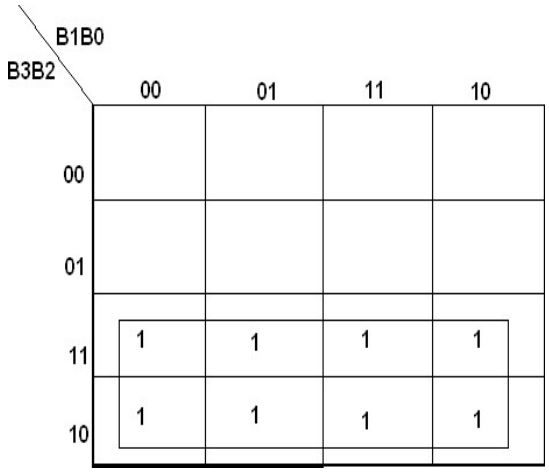
A two-level logic diagram may be obtained directly from the Boolean expressions derived by the maps. These are various other possibilities for a logic diagram that implements this circuit. Now the OR gate whose output is C+D has been used to implement partially each of three outputs.

Logic Diagram:

BINARY TO GRAY CODE CONVERTOR

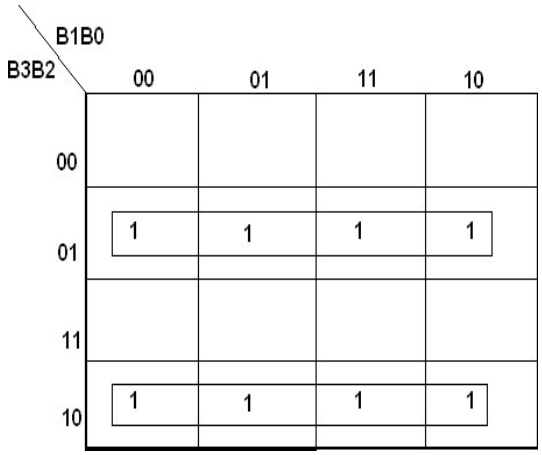


K-Map for G_3:



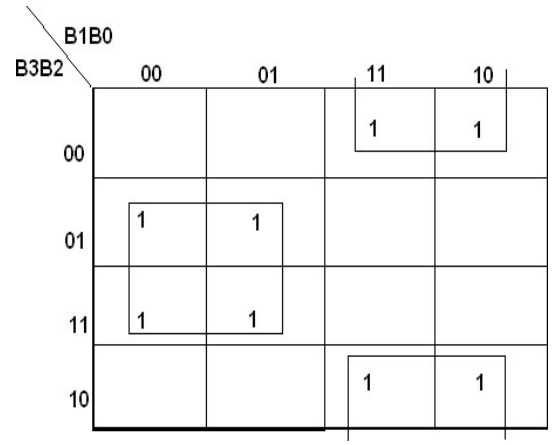
$G_3 = B_3$

K-Map for G_2:



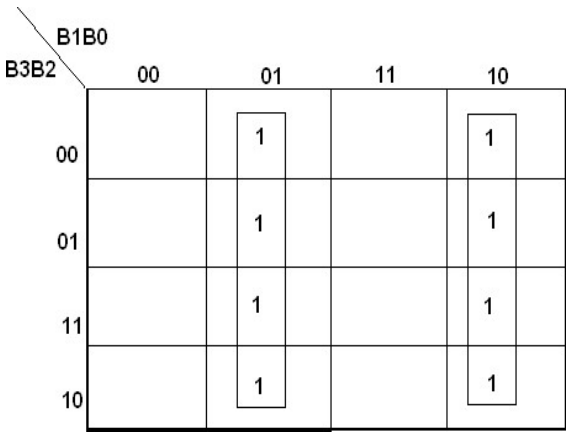
$G2 = B3 \oplus B2$

K-Map for G_1:



$G1 = B1 \oplus B2$

K-Map for G_0:



$G0 = B1 \oplus B0$

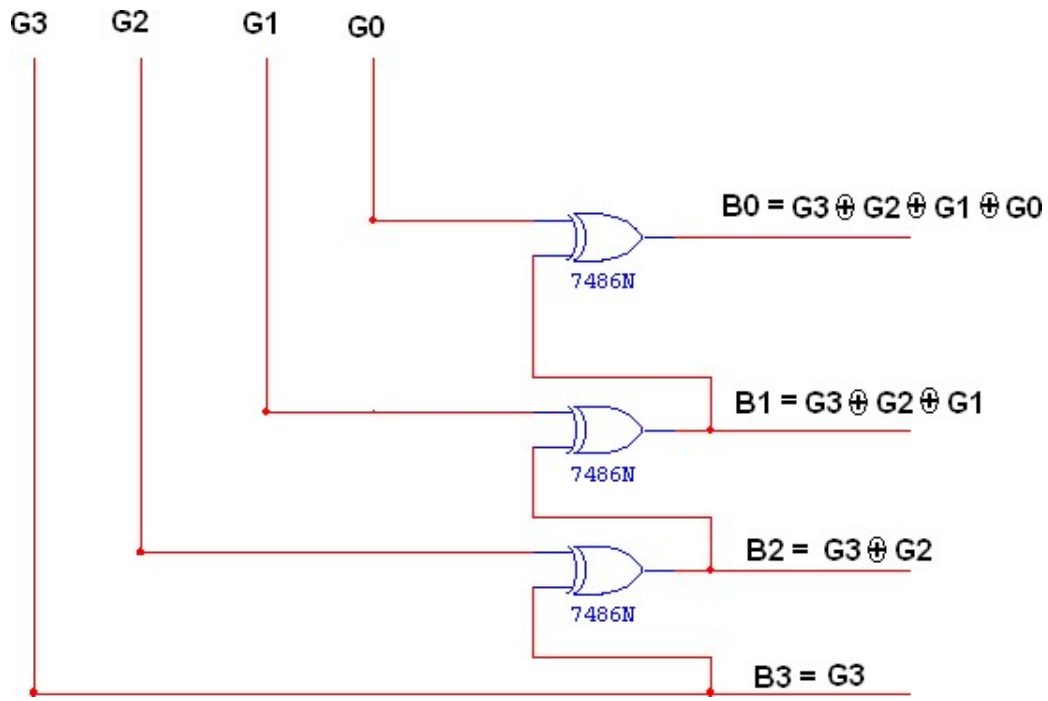
Truth Table:

| **Binary input** | **Gray code output** |

B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Logic Diagram:

GRAY CODE TO BINARY CONVERTOR



K-Map for B_3:

G3G2 \ G1G0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

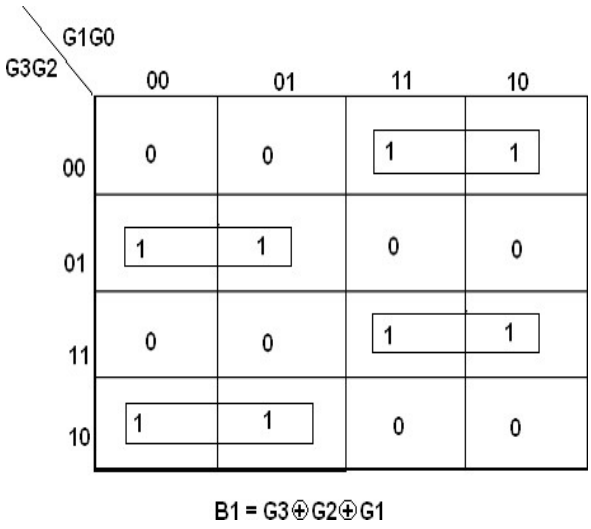
B3 = G3

K-Map for B_2:

G3G2 \ G1G0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

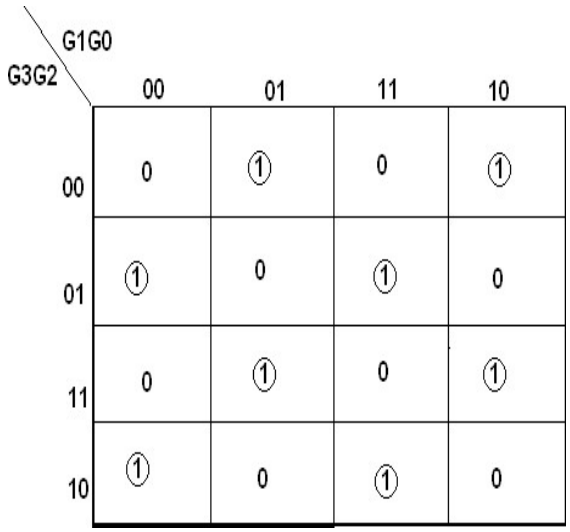
B2 = G3⊕G2

K-Map for B_1:



B1 = G3⊕G2⊕G1

K-Map for B_0:



B0 = G3⊕G2⊕G1⊕G0

Truth Table:

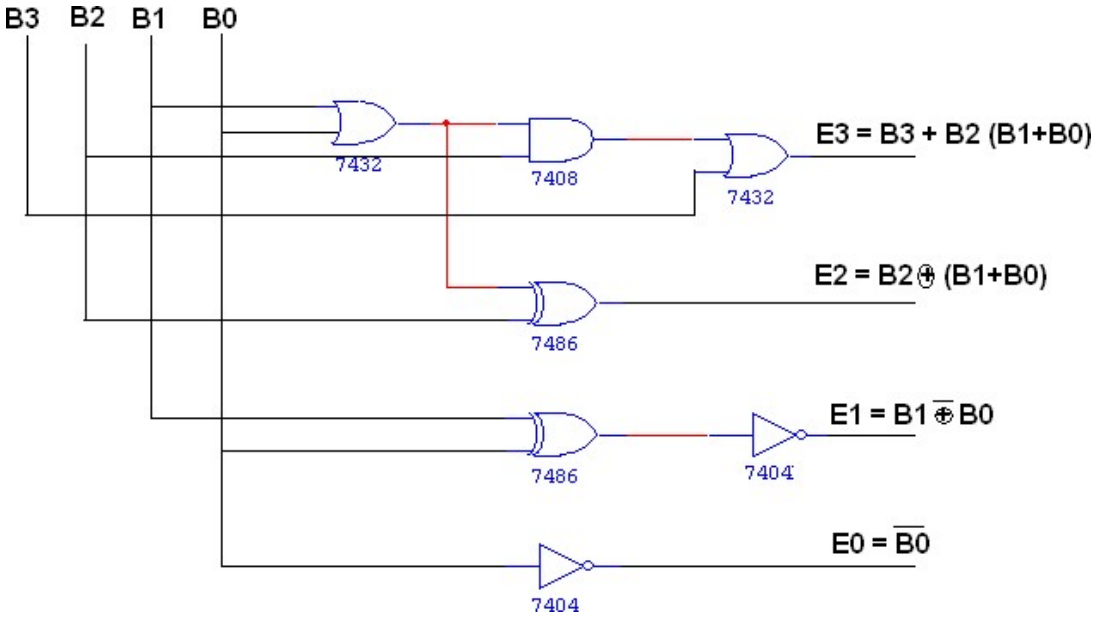
| **Gray Code** | **Binary Code** |

G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1

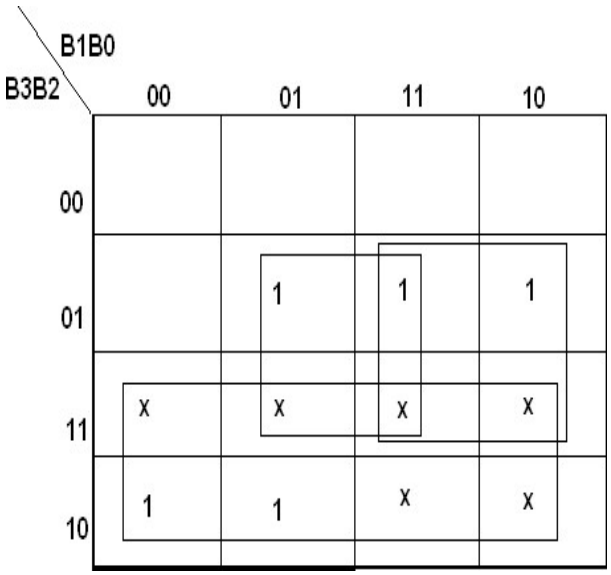
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Logic Diagram:

BCD TO EXCESS-3 CONVERTOR

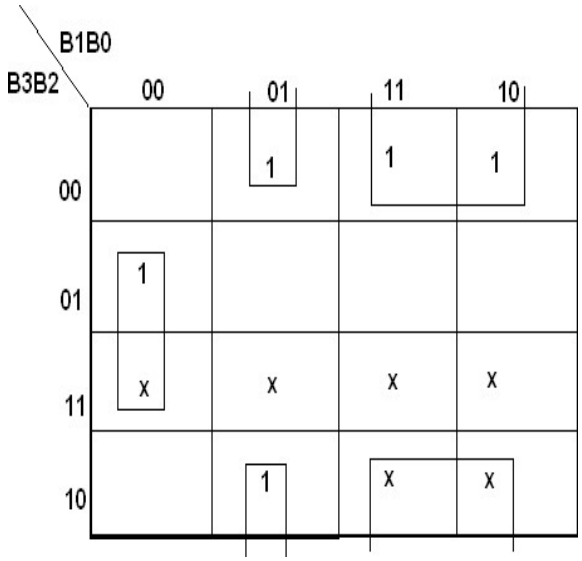


K-Map for E_3:



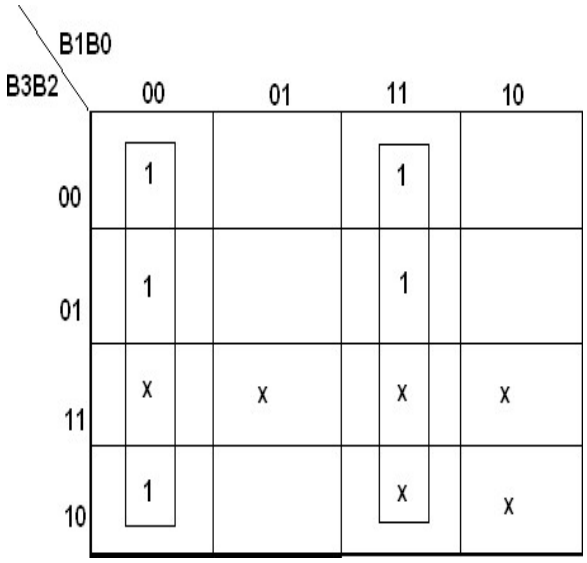
E3 = B3 + B2 (B0 + B1)

K-Map for E_2:



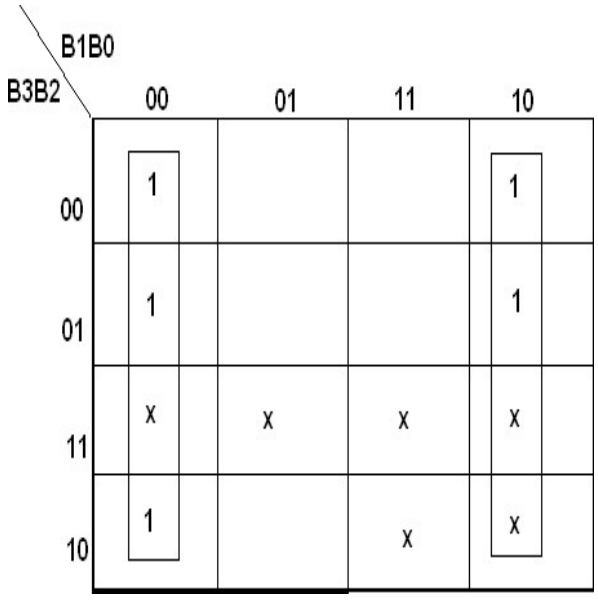
E2 = B2 ⊕ (B1 + B0)

K-Map for E_1:



E1 = B1 ⊕̄ B0

K-Map for E_0:



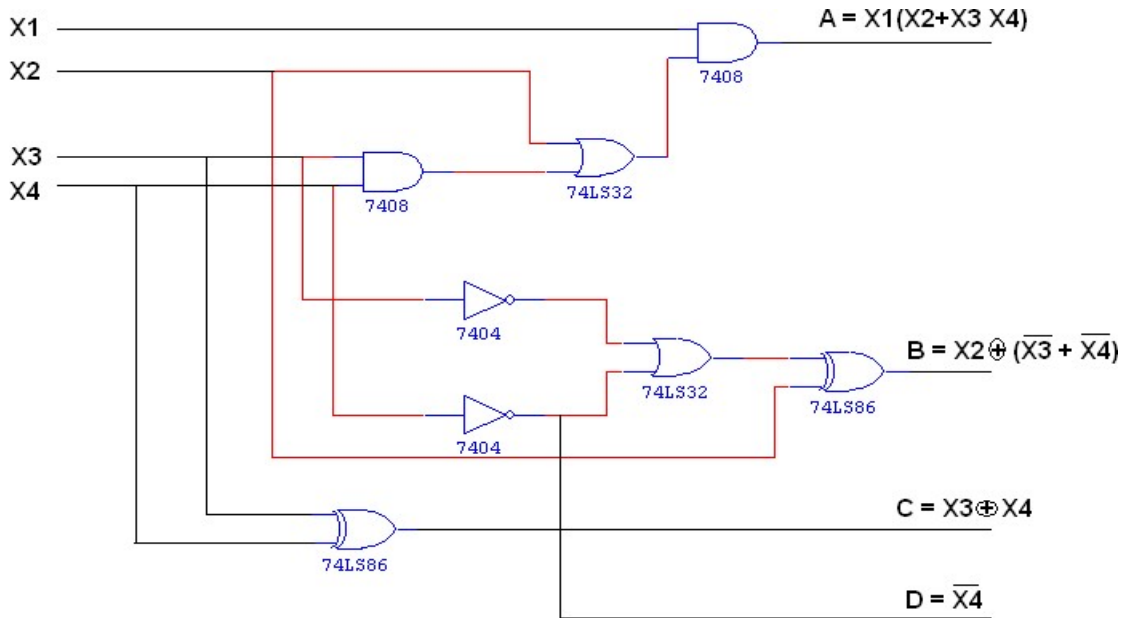
E0 = $\overline{B0}$

Truth Table:

BCD input				Excess – 3 output			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**
0	**0**	**0**	**1**	**0**	**1**	**0**	**0**
0	**0**	**1**	**0**	**0**	**1**	**0**	**1**
0	**0**	**1**	**1**	**0**	**1**	**1**	**0**
0	**1**	**0**	**0**	**0**	**1**	**1**	**1**
0	**1**	**0**	**1**	**1**	**0**	**0**	**0**
0	**1**	**1**	**0**	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**1**	**0**	**1**	**0**
1	**0**	**0**	**0**	**1**	**0**	**1**	**1**
1	**0**	**0**	**1**	**1**	**1**	**0**	**0**
1	**0**	**1**	**0**	**x**	**x**	**x**	**x**
1	**0**	**1**	**1**	**x**	**x**	**x**	**x**
1	**1**	**0**	**0**	**x**	**x**	**x**	**x**
1	**1**	**0**	**1**	**x**	**x**	**x**	**x**
1	**1**	**1**	**0**	**x**	**x**	**x**	**x**
1	**1**	**1**	**1**	**x**	**x**	**x**	**x**

Logic Diagram:

EXCESS-3 TO BCD CONVERTOR



K-Map for A:

X1 X2 \ X3 X4	00	01	11	10
00	X	X	0	X
01	0	0	0	0
11	1	X	X	X
10	0	0	1	0

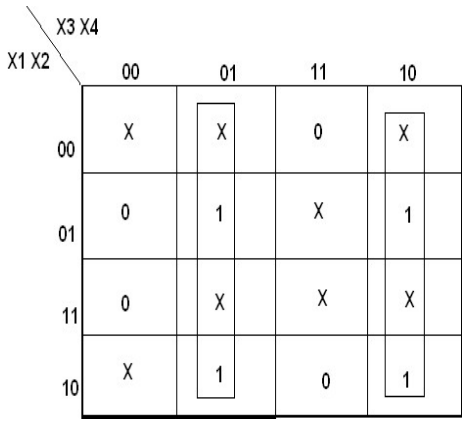
A = X1 X2 + X3 X4 X1

K-Map for B:

X1 X2 \ X3 X4	00	01	11	10
00	X	X	0	X
01	0	0	1	0
11	0	X	X	X
10	1	1	0	1

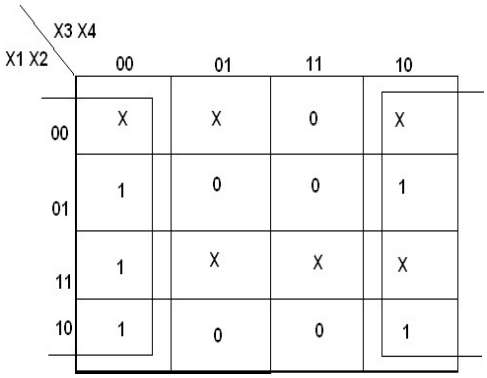
B = X2⊕ (X3 + X4)

K-Map for C:



$C = X3 \oplus X4$

K-Map for D:



$D = \overline{X4}$

Truth Table:

| **Excess – 3 Input** | **BCD Output** |

B3	B2	B1	B0	G3	G2	G1	G0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0

1	**0**	**1**	**0**	**0**	**1**	**1**	**1**
1	**0**	**1**	**1**	**1**	**0**	**0**	**0**
1	**1**	**0**	**0**	**1**	**0**	**0**	**1**

PROCEDURE:

(i) Connections were given as per circuit diagram.
(ii) Logical inputs were given as per truth table
(iii) Observe the logical output and verify with the truth tables.

Result:

Thus, binary to gray code converter, Gray to binary code converter, BCD to excess-3 code converter, Excess-3 to BCD code converter was implemented.

EXPERIMENT NO 8: DESIGN AND IMPLEMENTATION OF 4-BIT ADDER/ SUBTRACTOR AND BCD ADDER USING IC 7483

Aim:

To design and implement 4-bit adder / subtractor and BCD adder using IC 7483.

Apparatus Required:

Sl.No.	Component	Specification	Qty.
1.	IC	IC 7483	1
2.	EX-OR Gate	IC 7486	1
3.	NOT Gate	IC 7404	1
3.	IC Trainer Kit	-	1
4.	Patch Cords	-	40

Theory:

4 Bit Binary Adder:

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of next full adder in chain. The augends bits of 'A' and the addend bits of 'B' are designated by subscript numbers from right to left, with subscript 0 denoting the least significant bits. The carries are connected in chain through the full adder. The input carry to the adder is C_0 and it ripples through the full adder to the output carry C_4.

4 Bit Binary Subtractor:

The circuit for subtracting A-B consists of an adder with inverters, placed between each data input 'B' and the corresponding input of full adder. The input carry C_0 must be equal to 1 when performing subtraction.

4 Bit Binary Adder/Subtractor:

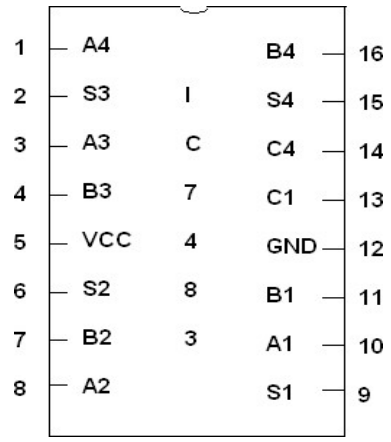
The addition and subtraction operation can be combined into one circuit with one common binary adder. The mode input M controls the operation. When M=0, the circuit is adder circuit. When M=1, it becomes subtractor.

4 Bit BCD Adder:

Consider the arithmetic addition of two decimal digits in BCD, together with an input carry from a previous stage. Since each input digit does not exceed 9, the output sum cannot be greater than 19, the 1 in the sum being an input carry. The output of two decimal digits must be represented in BCD and should appear in the form listed in the columns.

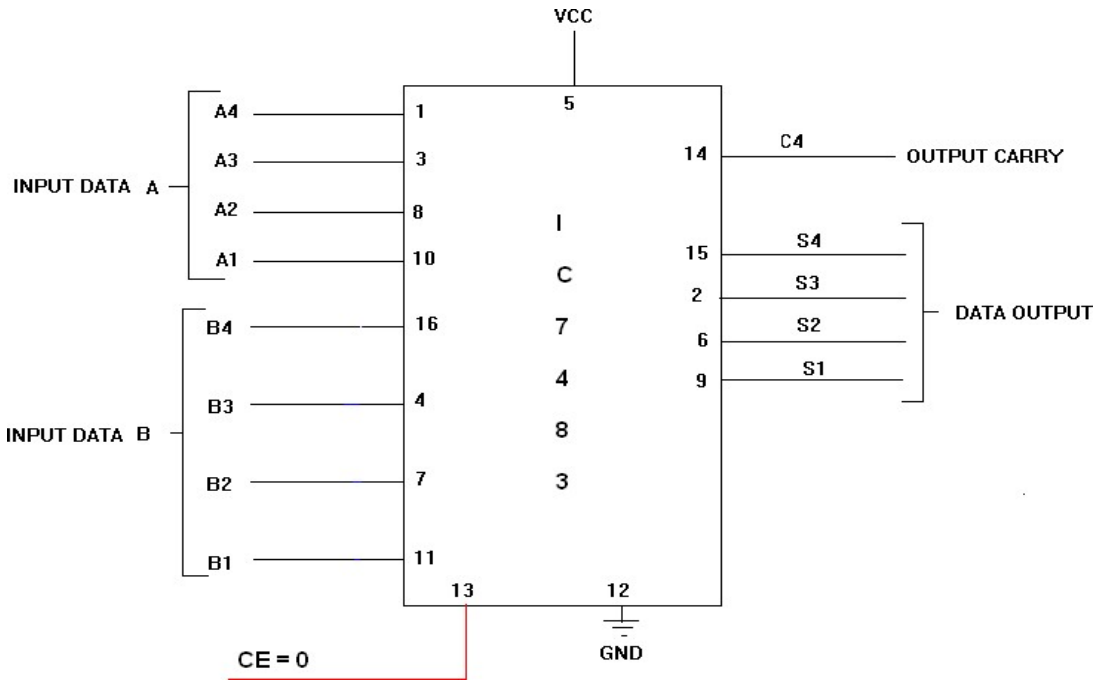
ABCD adder that adds 2 BCD digits and produce a sum digit in BCD. The 2 decimal digits, together with the input carry, are first added in the top 4 bit adder to produce the binary sum.

Pin Diagram for IC 7483:

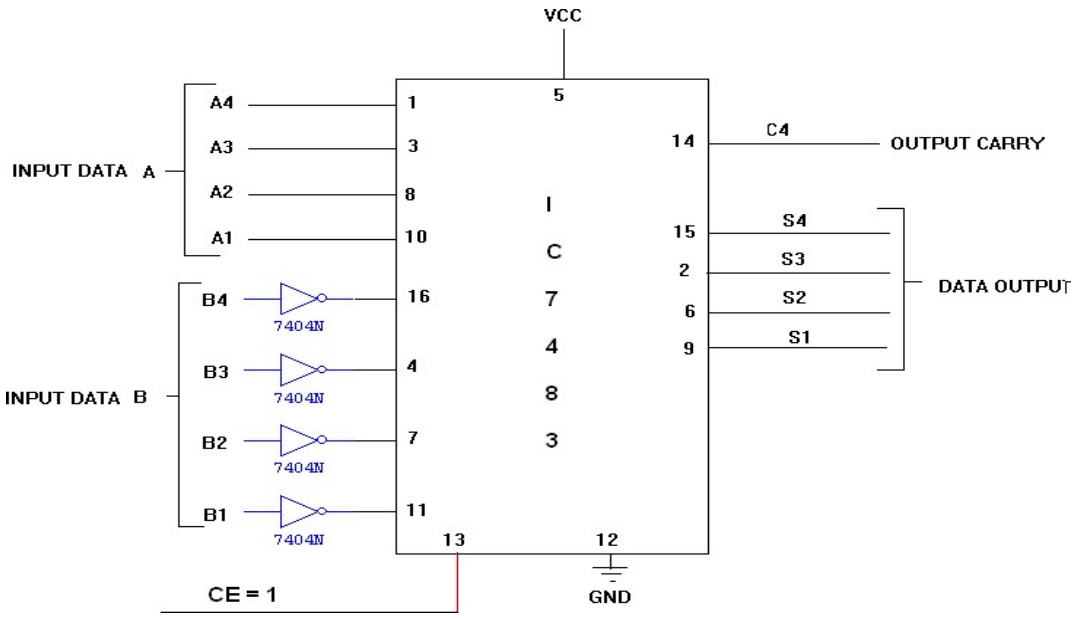


Logic Diagram:

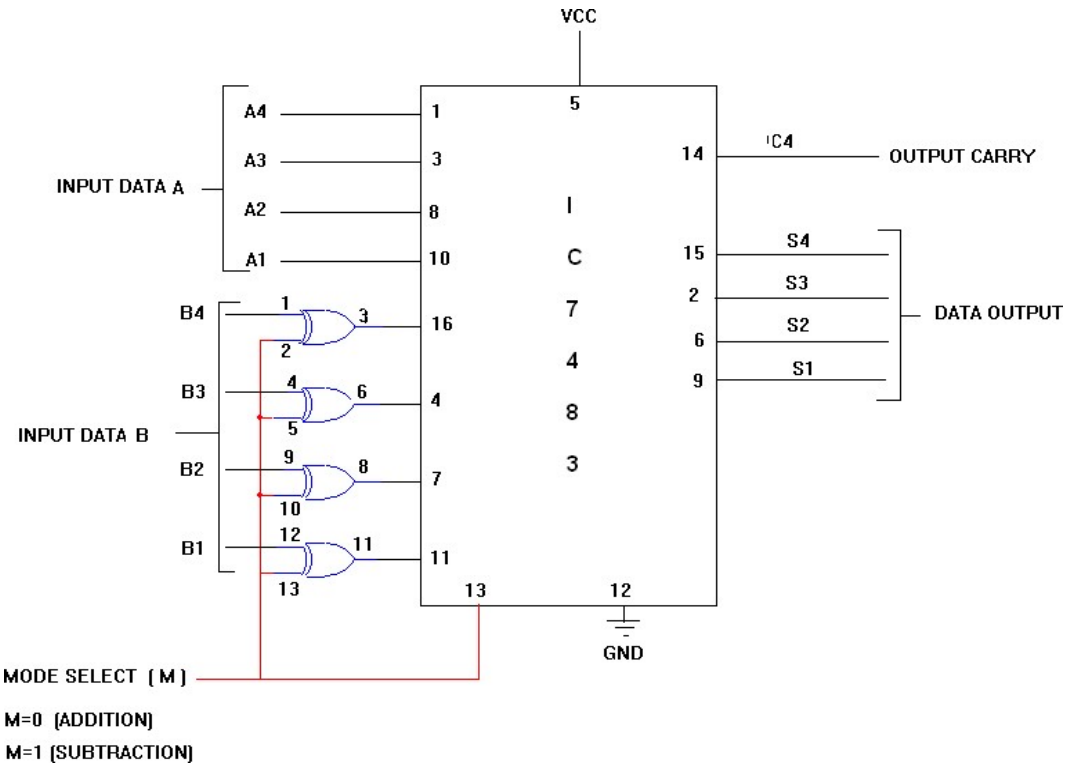
4-Bit Binary Adder



4-Bit Binary Subtractor



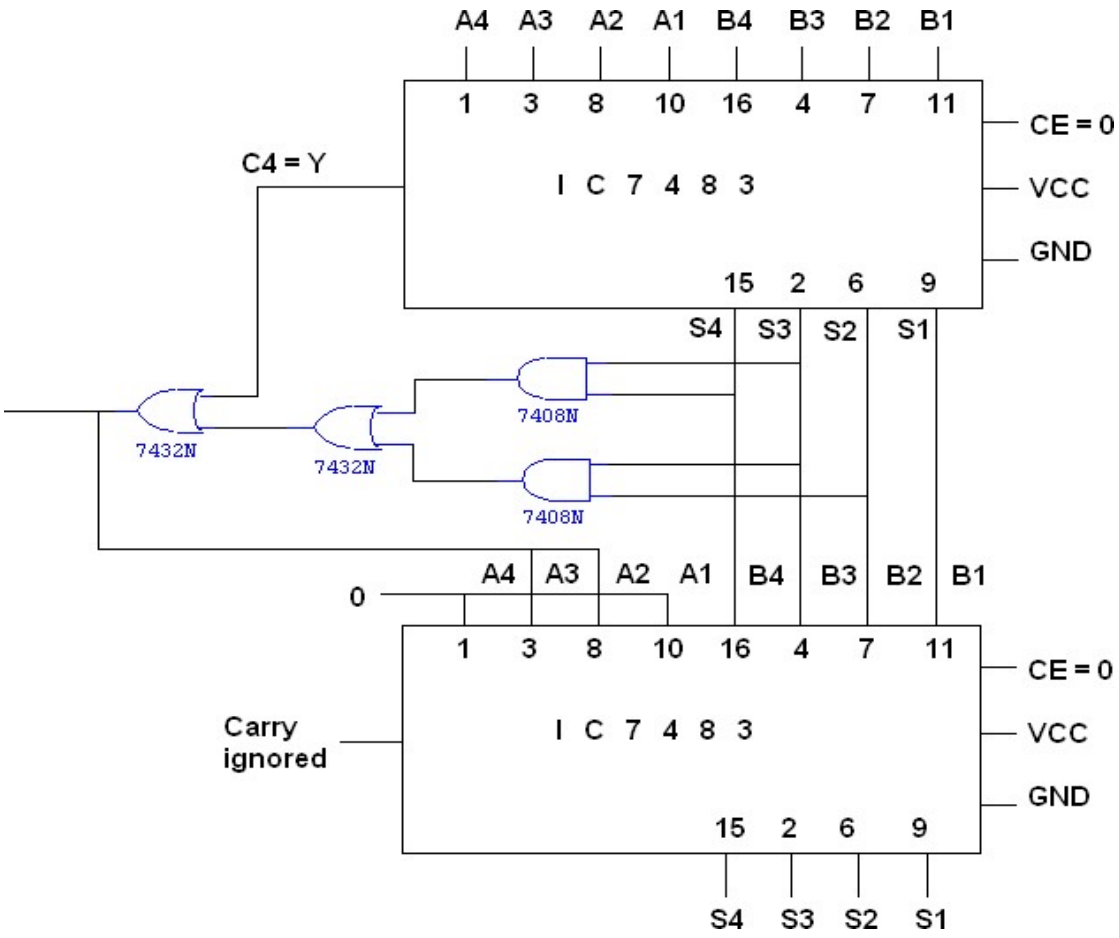
4-Bit Binary Adder/Subtractor



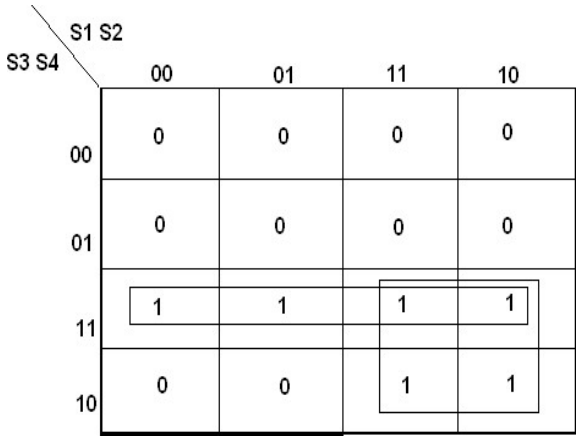
Truth Table:

Input Data A				Input Data B				Addition					Subtraction				
A4	A3	A2	A1	B4	B3	B2	B1	C	S4	S3	S2	S1	B	D4	D3	D2	D1
1	0	0	0	0	0	1	0	0	1	0	1	0	1	0	1	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	0	1	0	0	1	1	1	1
1	1	1	0	1	1	1	1	1	1	0	1	0	0	1	1	1	1
1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	1	0	1

BCD ADDER



K- MAP



Y = S4 (S3 + S2)

Truth Table:

BCD SUM				CARRY
S4	S3	S2	S1	C
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

PROCEDURE:

(i) Connections were given as per circuit diagram.
(ii) Logical inputs were given as per truth table
(iii) Observe the logical output and verify with the truth tables.

Result:

Thus, the 4-bit adder / subtractor and BCD adder using IC 7483 was designed and implement.

EXPERIMENT NO 9: DESIGN AND IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER

Aim:

To design and implement multiplexer and De-multiplexer using logic gates and study of IC 74150 and IC 74154.

Apparatus Required:

Sl.No.	Component	Specification	Qty.
1.	3 I/P AND GATE	IC 7411	2
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	32

Theory:

MULTIPLEXER:

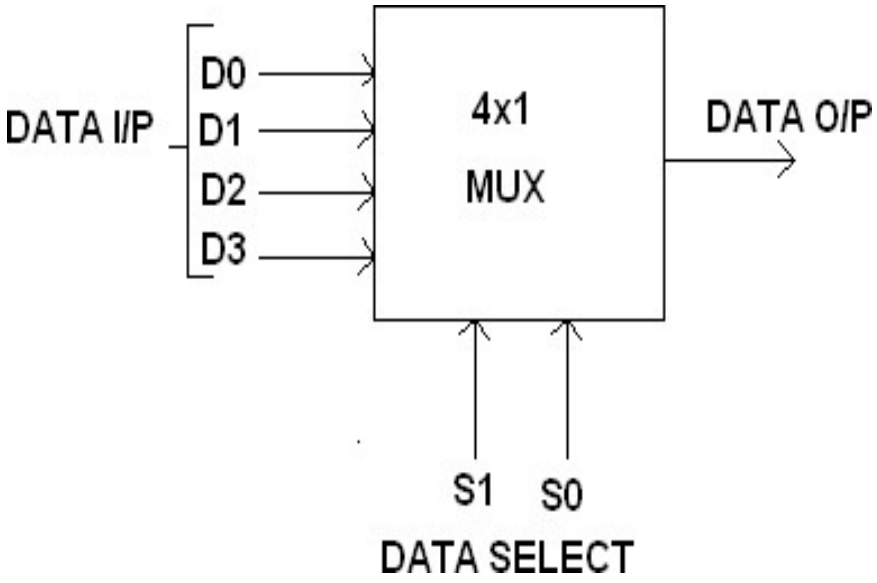
Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input line and n selection lines whose bit combination determine which input is selected.

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

Block Diagram for 4:1 Multiplexer:

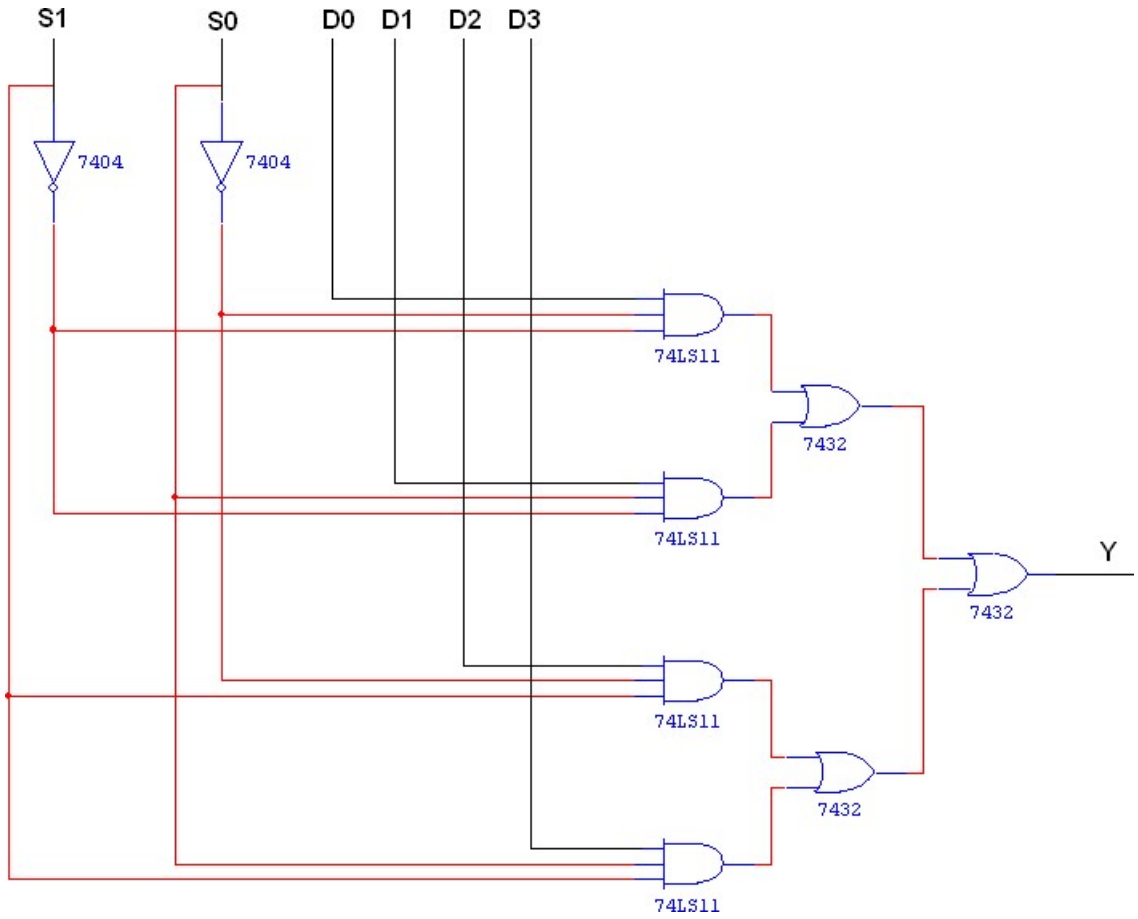


Function Table:

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

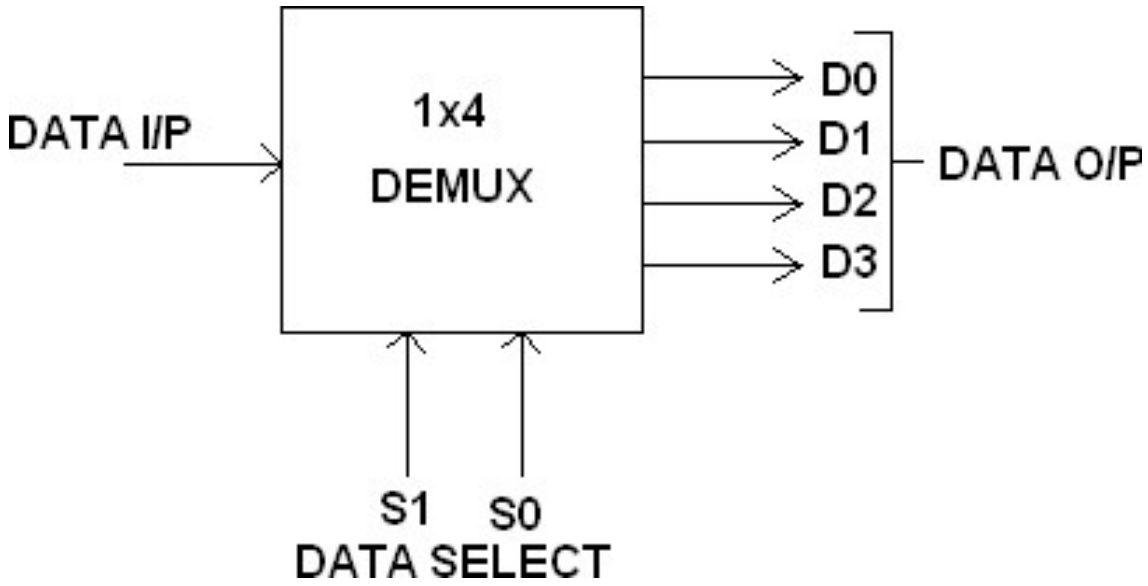
Circuit Diagram For Multiplexer:



Truth Table:

S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Block Diagram for 1:4 Demultiplexer:

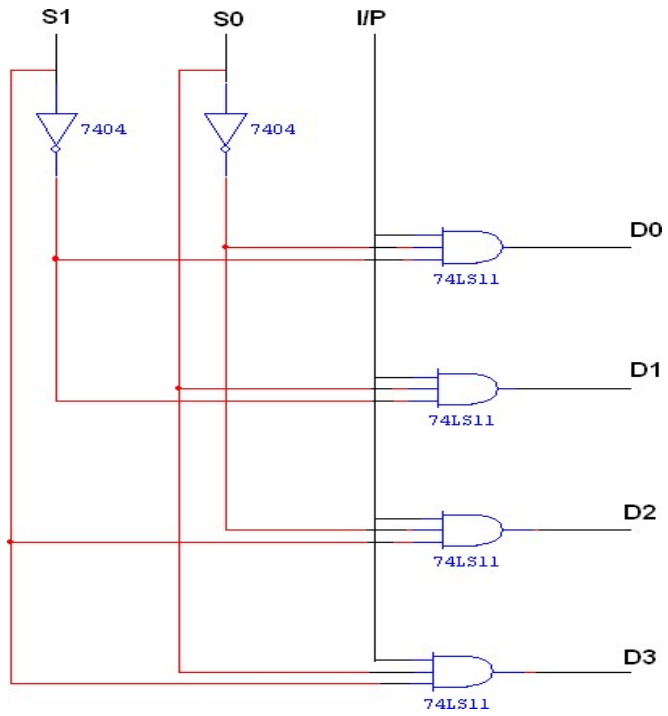


Function Table

S1	S0	INPUT
0	0	X → D0 = X S1' S0'
0	1	X → D1 = X S1' S0
1	0	X → D2 = X S1 S0'
1	1	X → D3 = X S1 S0

Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0

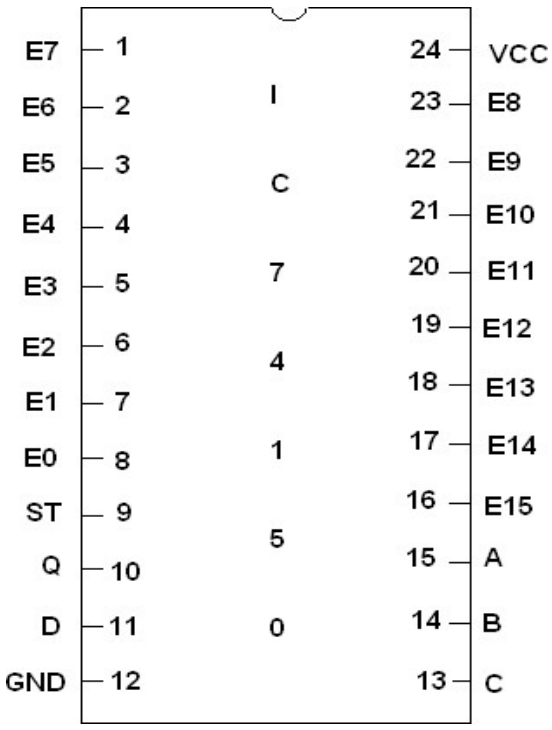
Logic Diagram for Demultiplexer:



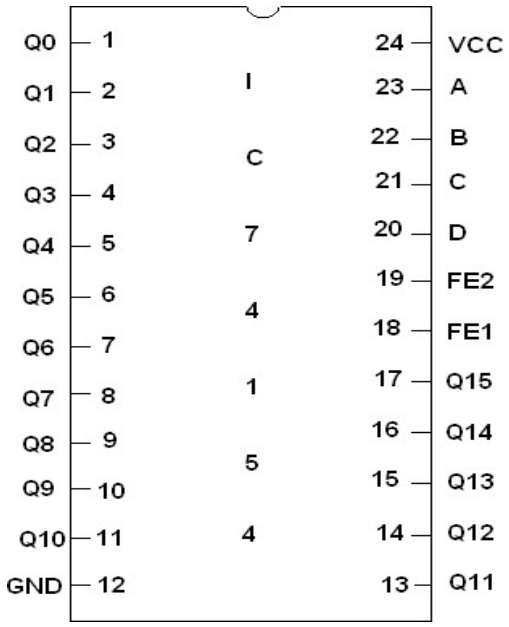
Truth Table:

INPUT			OUTPUT			
S1	S0	I/P	D0	D1	D2	D3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

Pin Diagram for IC 74150:



Pin Diagram for IC 74154:



Procedure:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

Result:

Thus, the multiplexer and De-multiplexer was designed using logic gates and implement.

EXPERIMENT NO 10: DESIGN AND IMPLEMENTATION OF ENCODER AND DECODER

Aim:

To design and implement encoder and decoder using logic gates and study of IC 7445 and IC 74147.

Apparatus Required:

Sl.No.	Component	Specification	Qty.
1.	3 I/P NAND Gate	IC 7410	2
2.	OR Gate	IC 7432	3
3.	NOT Gate	IC 7404	1
2.	IC Trainer Kit	-	1
3.	Patch Cords	-	27

Theory:

Encoder:

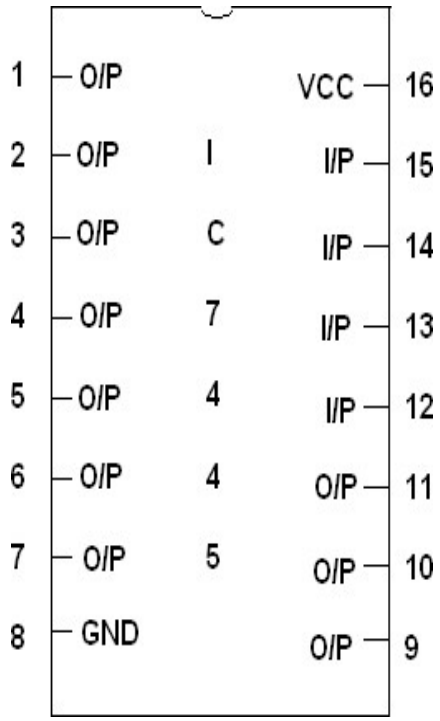
An encoder is a digital circuit that perform inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generates the binary code corresponding to the input value. In octal to binary encoder it has eight inputs, one for each octal digit and three output that generate the corresponding binary code. In encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguila that when all inputs are zero the outputs are zero. The zero outputs can also be generated when D0 = 1.

Decoder:

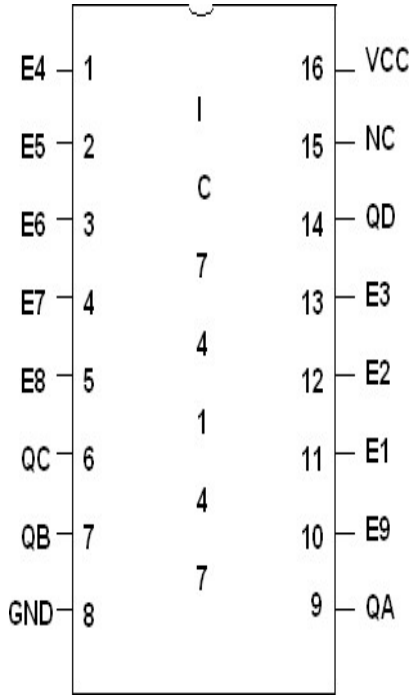
A decoder is a multiple input multiple output logic circuit which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e there is one to one mapping can be expressed in truth table. In the block diagram of decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through out $2^n - 1$.

PIN Diagram for IC 7445:

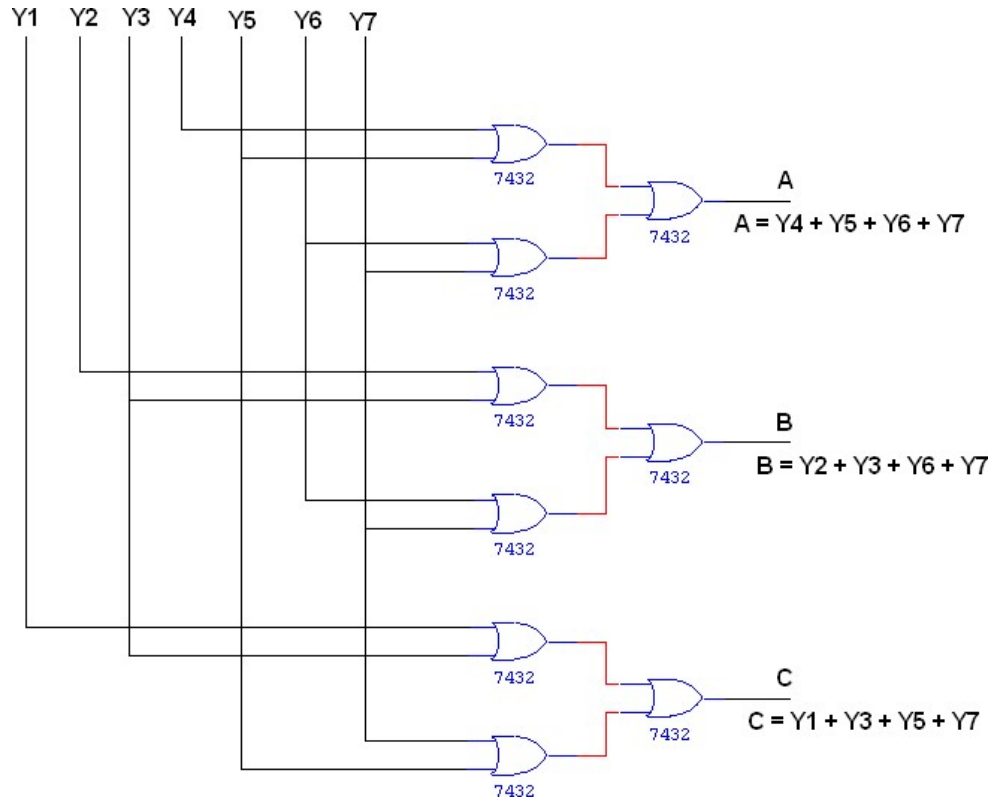
BCD to Decimal Decoder:



PIN Diagram for IC 74147:



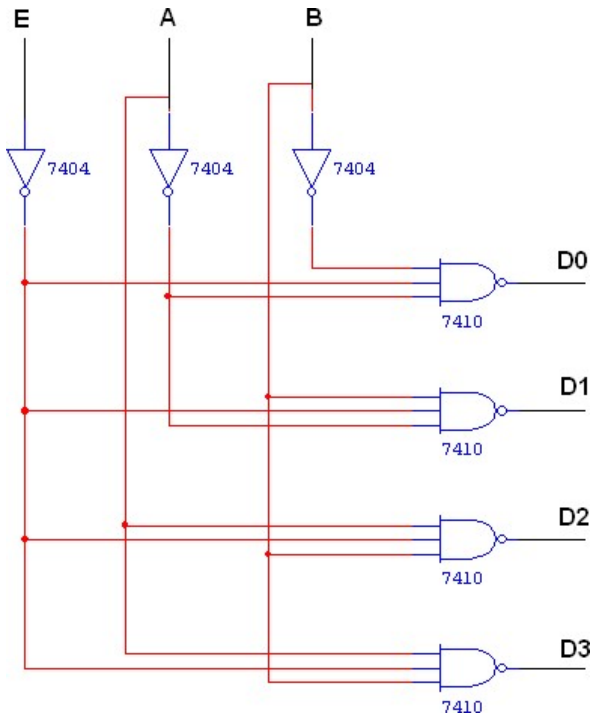
Logic Diagram for Encoder:



Truth Table:

INPUT							OUTPUT		
Y1	Y2	Y3	Y4	Y5	Y6	Y7	A	B	C
1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	1	1	1	1

Logic Diagram for Decoder:



Truth Table:

INPUT			OUTPUT			
E	**A**	**B**	**D0**	**D1**	**D2**	**D3**
1	**0**	**0**	**1**	**1**	**1**	**1**
0	**0**	**0**	**0**	**1**	**1**	**1**
0	**0**	**1**	**1**	**0**	**1**	**1**
0	**1**	**0**	**1**	**1**	**0**	**1**
0	**1**	**1**	**1**	**1**	**1**	**0**

Procedure:

(iv) Connections are given as per circuit diagram.
(v) Logical inputs are given as per circuit diagram.
(vi) Observe the output and verify the truth table.

Result:

Thus, the encoder and decoder were designed using logic gates and implement.

EXPERIMENT NO 11: DESIGN AND IMPLEMENTATION OF 3 BIT SYNCHRONOUS UP/DOWN COUNTER

Aim:

To design and implement 3 bit synchronous up/down counter.

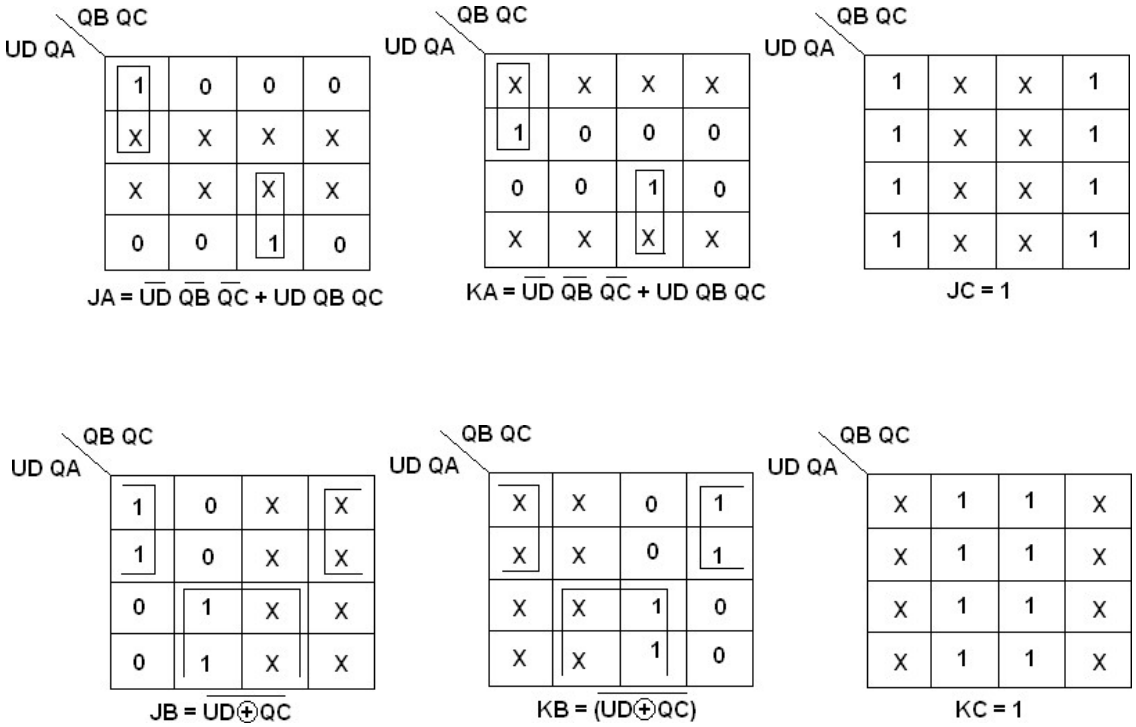
Apparatus Required:

Sl.No.	Component	Specification	Qty.
1.	JK FLIP FLOP	IC 7476	2
2.	3 I/P AND GATE	IC 7411	1
3.	OR GATE	IC 7432	1
4.	XOR GATE	IC 7486	1
5.	NOT GATE	IC 7404	1
6.	IC TRAINER KIT	-	1
7.	PATCH CORDS	-	35

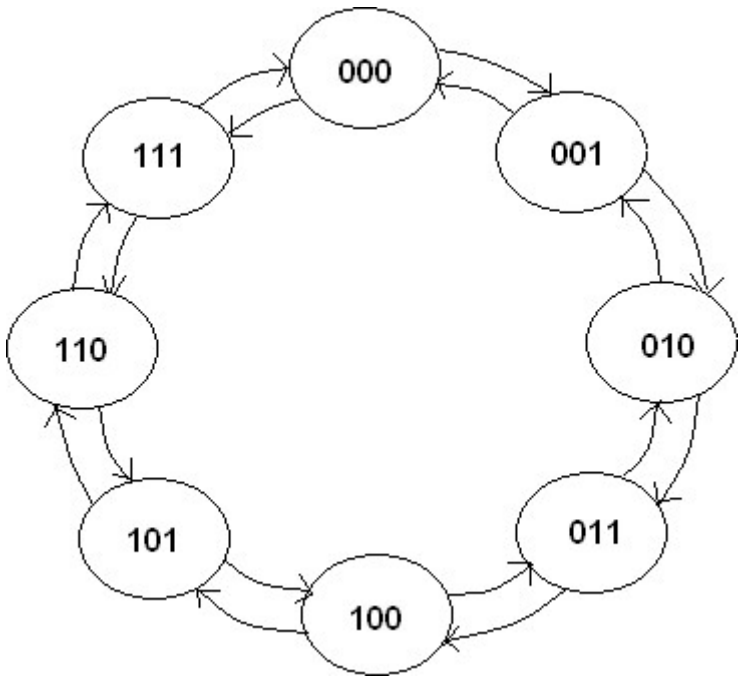
Theory:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

K- MAP



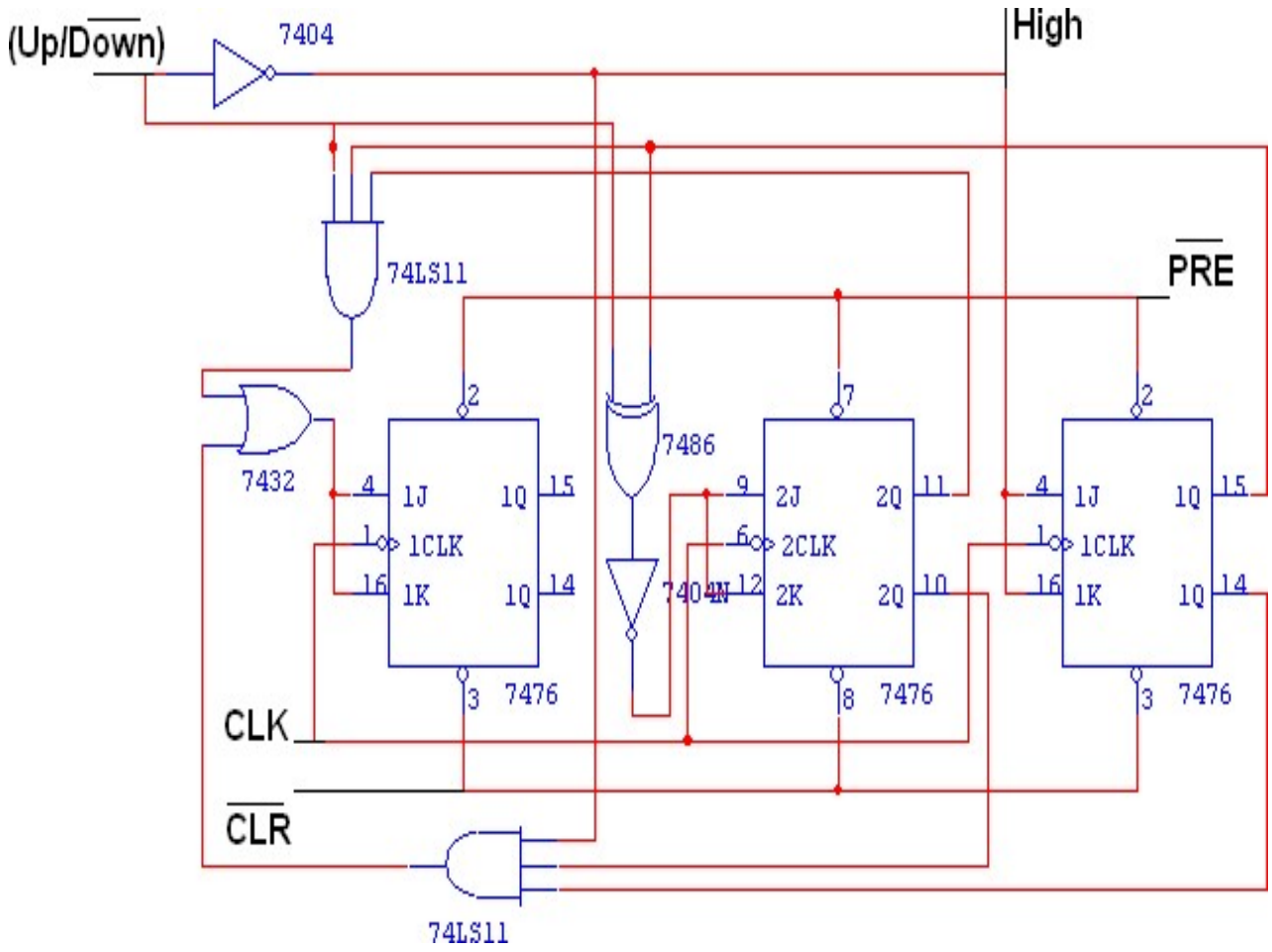
State Diagram:



Characteristics Table:

Q	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Logic Diagram:



Truth Table:

Input	Present State			Next State			A		B		C	
Up/Down	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	1	1	1	X	1	X	1	X
0	1	1	1	1	1	0	X	0	X	0	X	1
0	1	1	0	1	0	1	X	0	X	1	1	X
0	1	0	1	1	0	0	X	0	0	X	X	1
0	1	0	0	0	1	1	X	1	1	X	1	X
0	0	1	1	0	1	0	0	X	X	0	X	1
0	0	1	0	0	0	1	0	X	X	1	1	X
0	0	0	1	0	0	0	0	X	0	X	X	1
1	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
1	0	1	0	0	1	1	0	X	X	0	1	X
1	0	1	1	1	0	0	1	X	X	1	X	1
1	1	0	0	1	0	1	X	0	0	X	1	X
1	1	0	1	1	1	0	X	0	1	X	X	1
1	1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	0	0	X	1	X	1	X	1

Procedure:

(vii) Connections are given as per circuit diagram.
(viii) Logical inputs are given as per circuit diagram.
(ix) Observe the output and verify the truth table.

Result:

Thus, 3 bit synchronous up/down counter was designed and implemented.