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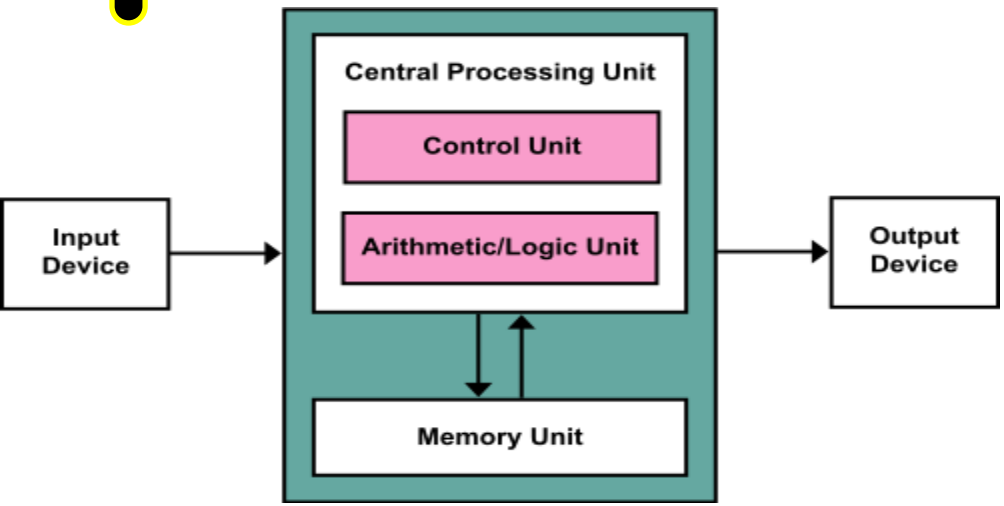
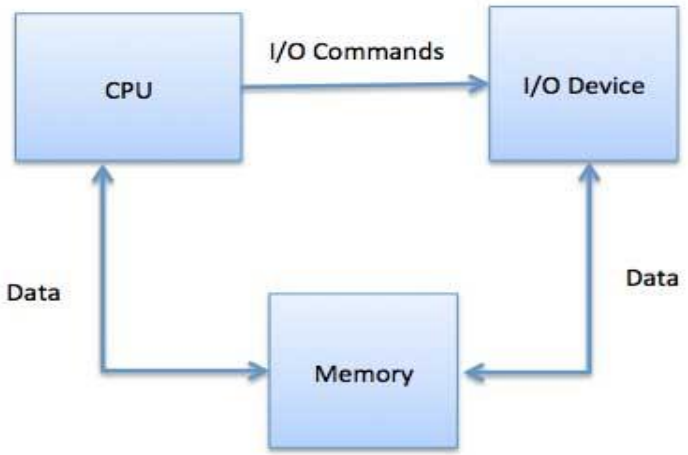
CHAPTER -7
I/O MANAGEMENT AND DISK SCHEDULING

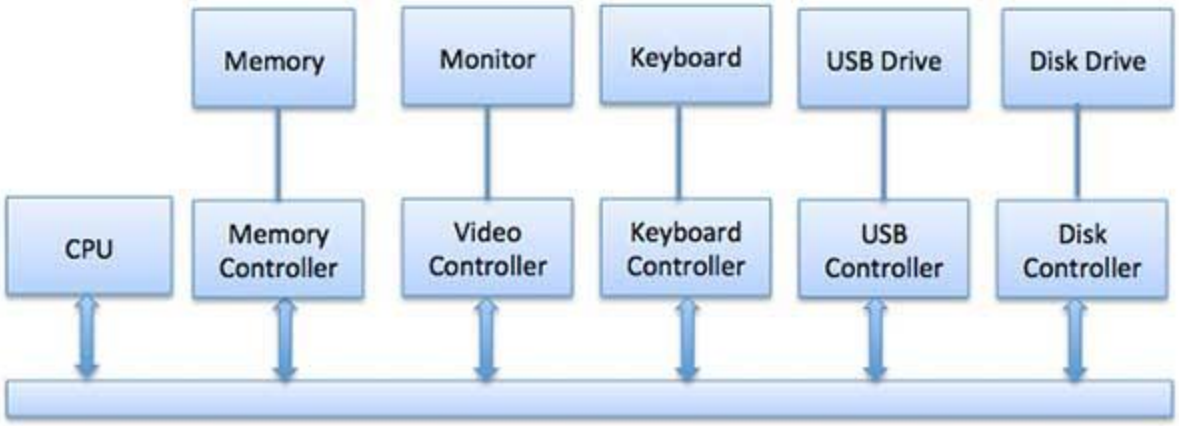




Subject:- OS **Code:-3140702**	**Prepared by:** **Asst.Prof.Foram Patel** **(Computer Department,ACET)**	AMIRAJ COLLEGE OF ENGINEERING & TECHNOLOGY

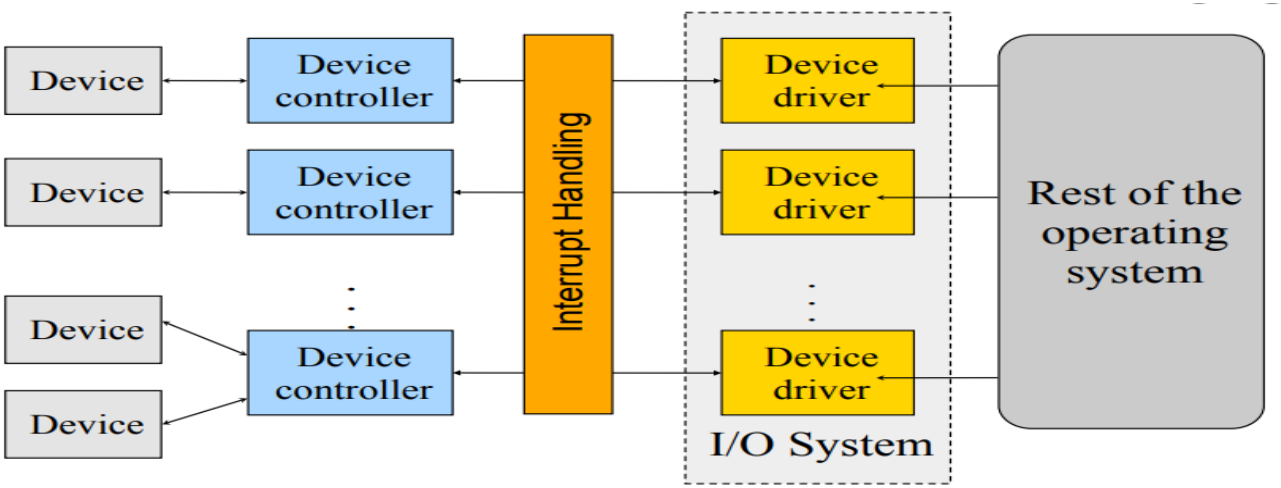
I/O DEVICE

- **I/O Device:**
- IO device, an input/output device is any hardware used by a human operator or other systems to communicate with a computer.
- Sending data (output) to a computer and receiving data from a computer (input).



- CD-R/RW, DVD, and Blu-ray drive
- Digital camera
- Floppy diskette drive
- Hard drives
- Modem
- Network adapter
- SD Card
- Touch screen

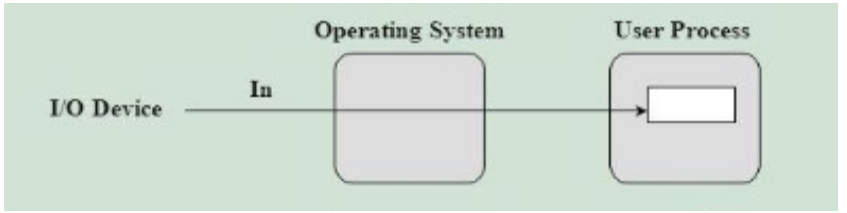
I/O DRIVER



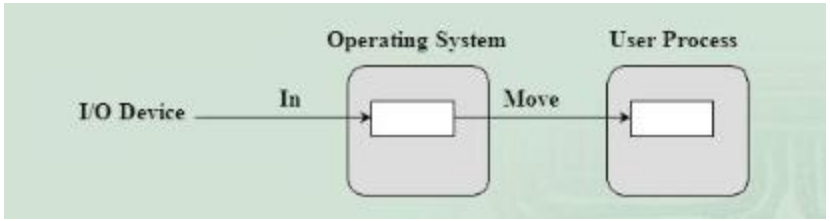
- Manage the I/O devices.
- Driver initialize devices.
- Manage data transfer
- Accept and process interrupts.
- Maintain the integrity of driver and kernel.
- Schedule multiple requests.

I/O BUFFERING

- **I/O buffering:**
- The process of temporarily storing data that is passing between a processor and a peripheral.
- **No buffering:**
- Data transferred from (to) user directly to (from) device.
- Each read or write causes an actual I/O operation.
- **Single buffering:**
- When a user process issues an I/O request, the O.S assigns a buffer in the system portion of main memory to the operation



NO BUFFERING



SINGLE BUFFERING

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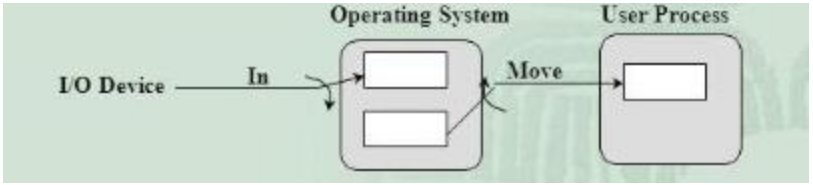
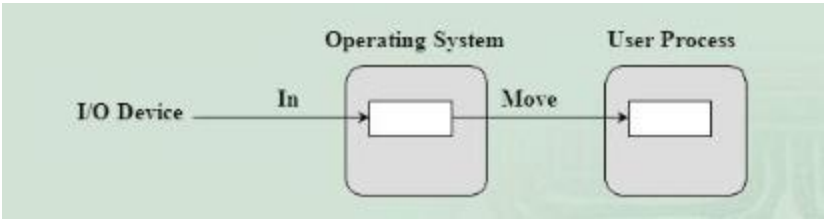
I/O BUFFERING

- **Double buffering:**
- Use two system buffers instead of one.
- A process can transfer data to or from one buffer while operating system fills the other duffer.
- **Circular buffering:**
- More than two buffers are used.
- Each individual buffer is one unit.
- When more than two buffers are used, the collection of buffers is itself reffered to as circular buffer with each individual buffer being one unit.



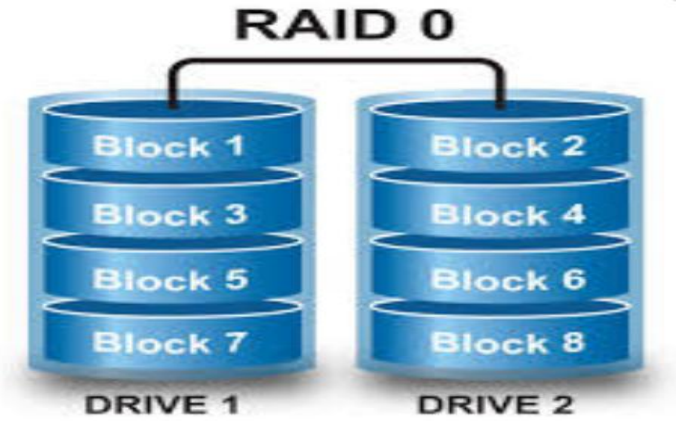
DOUBLE BUFFERING

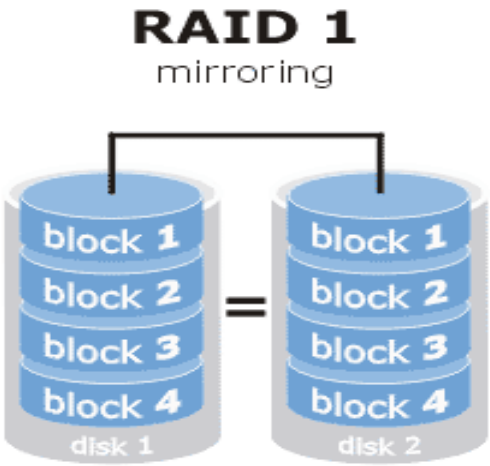


CIRCULAR BUFFERING

(REDUNDANT ARRAY OF INDEPENDENT DISKS)

- **Level 0:**
- This configuration has striping, but no redundancy of data.
- It does not provide fault tolerance.
- **Level 1:**
- Also known as disk mirroring.
- Two drives duplicate the storage of data.
- There is no striping.
- Increases read performance.
- It reads and writes the exact same data to each disk.





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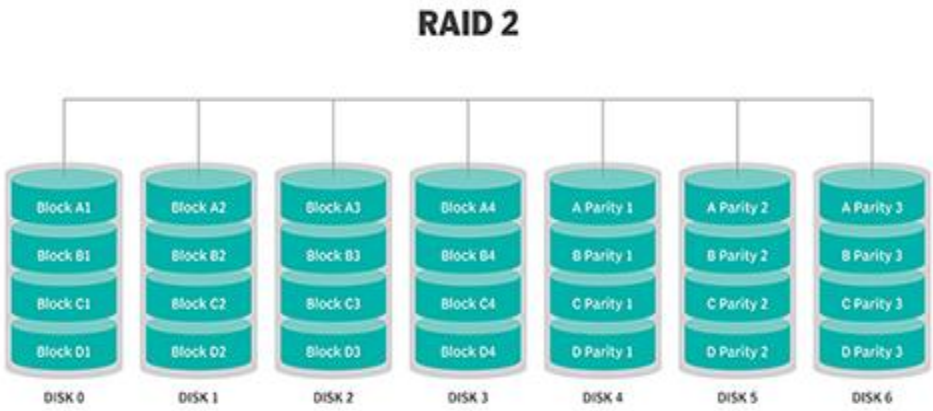
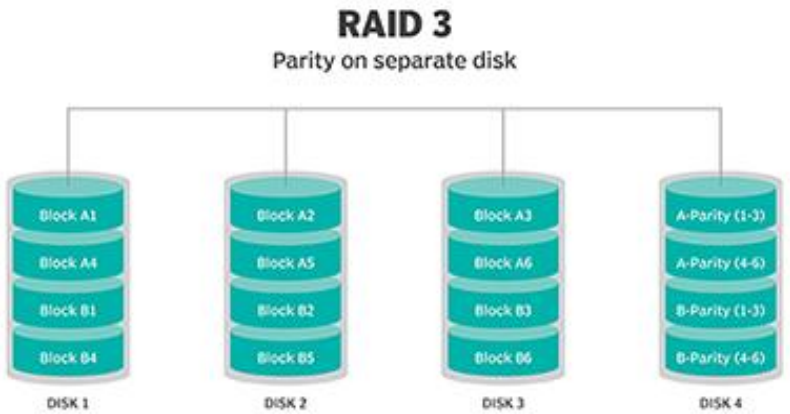
(REDUNDANT ARRAY OF INDEPENDENT DISKS)

- **Level 2:**
- This configuration uses striping across disks.
- some disks storing error checking and correcting (ECC) information.
- It uses a dedicated Hamming code parity.
- **Level 3:**
- It uses striping and dedicates one drive to storing parity information.
- It cannot overlap I/O.
- ECC information is used to detect errors





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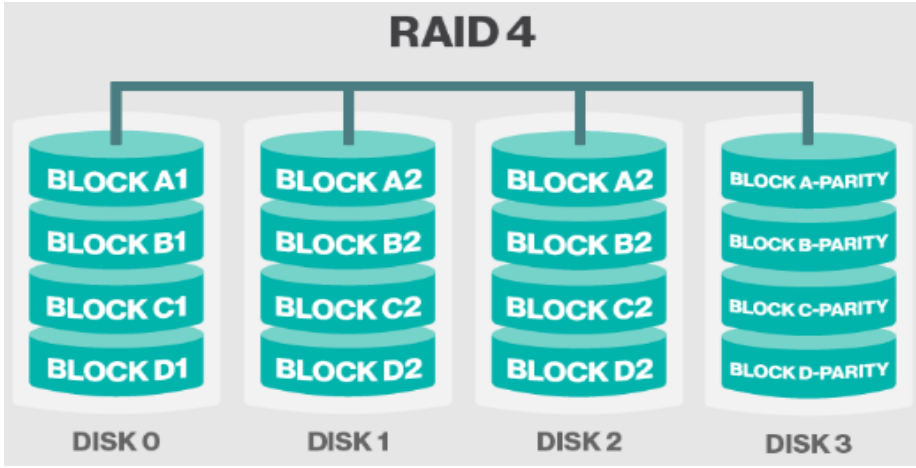
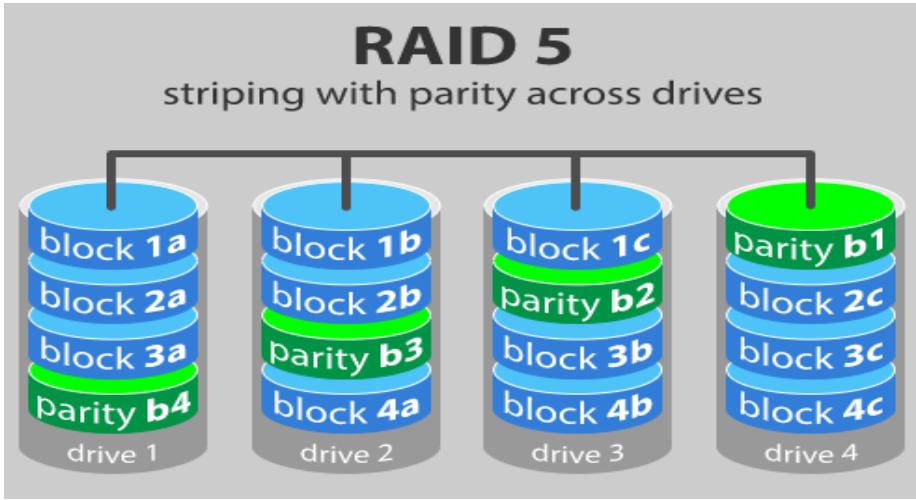
(REDUNDANT ARRAY OF INDEPENDENT DISKS)

- **Level 4:**
- RAID 4 is very similar to RAID 3.
- This level uses large stripes.
- RAID 4 does not strip data at block levels
- All write operations are required to update the parity drive.
- **Level 5:**
- This level is based on parity block-level striping.
- RAID 5 requires at least three disks.
- When a disk fails, it can take a long time to rebuild a RAID 5 array.





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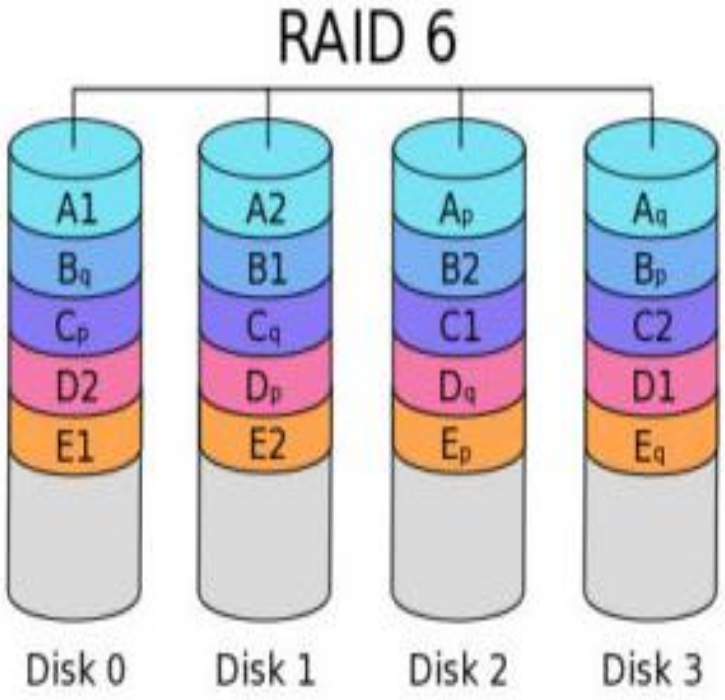
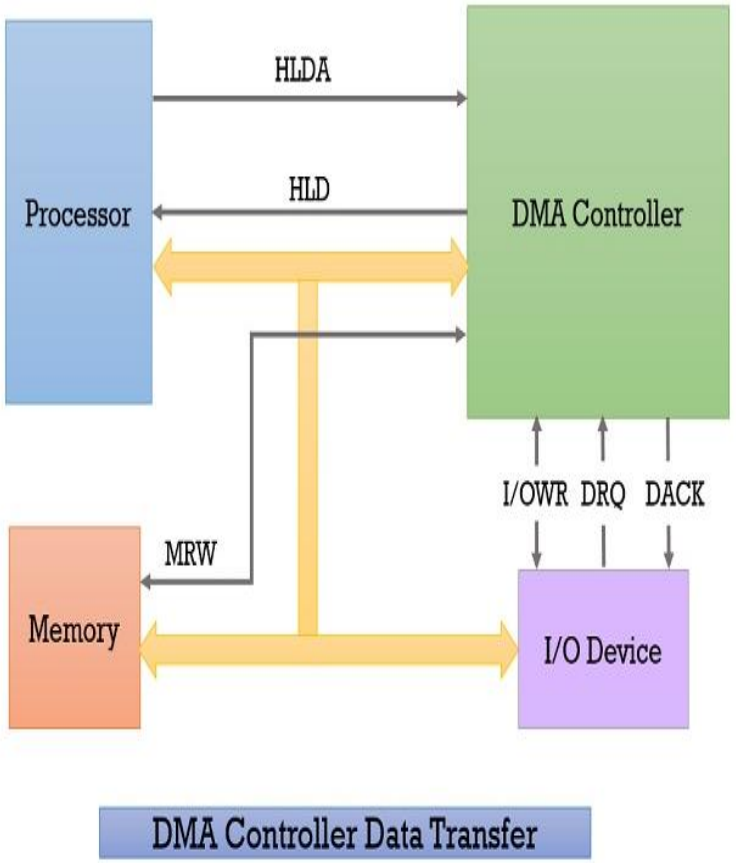
(REDUNDANT ARRAY OF INDEPENDENT DISKS)

- **Level 6:**
- Also known as double-**parity** RAID.
- This RAID level operates like RAID 5 with distributed parity and striping.
- A second parity scheme distributed across the drives in the array.
- RAID 6 arrays often have slower write performance than RAID 5 arrays.
- The system stores an additional parity block on each desk.
- The main operational difference in RAID 6 is that there is a minimum of four disks in a RAID 6 array.



DIRECT MEMORY ACCESS

- I/O device send to and from memory, DMA request DRQ to the DMA controller. DMA controller asks CPU to send the Hold request (HLD).
- CPU receives HLD from DMA controller and relinquishes the bus and sends HLDA to DMA controller.
- DMA controller acknowledges I/O device (DACK) that the data transfer can be performed and DMA controller takes the charge of the system bus and transfers the data to or from memory.



DMA Controller Data Transfer