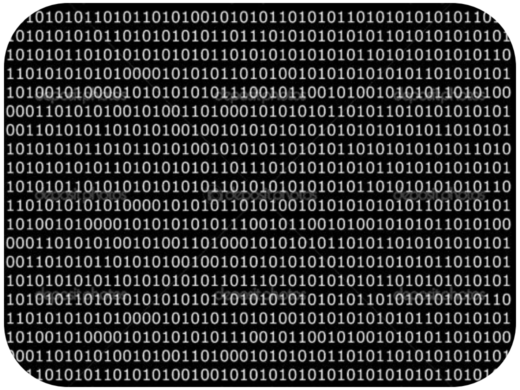
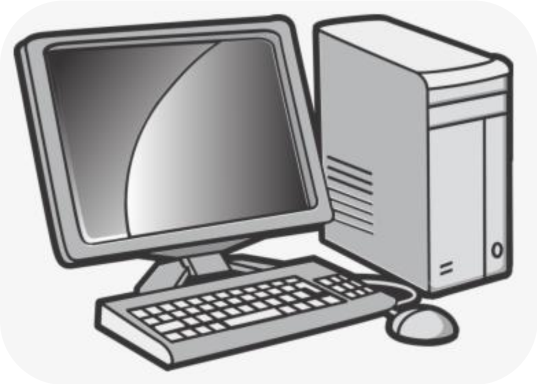
AMIRAJ

COLLEGE OF ENGINEERING & TECHNOLOGY

Unit-7
Computer Arithmetic





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Topics to be covered

- Introduction,
- Addition and subtraction Algorithms
- Multiplication Algorithms

  (Booth Multiplication Algorithm)
- Division Algorithms
- Floating Point Arithmetic operations
- Decimal Arithmetic Unit

Introduction

- What are arithmetic instructions- that manipulate data to produce results for solutions of computational problems.
- The basic arithmetic operations- addition subtraction, multiplication and division
- The arithmetic instructions may specify - binary / decimal data- can be fixed point or floating point.
- Negative numbers may be in signed magnitude form.

Introduction

3 ways of representing negative fixed point binary numbers:

- Signed-magnitude representation
- Signed-1’s complement
- Signed -2’s complement—Most computers use this form for performing arithmetic operation with integers

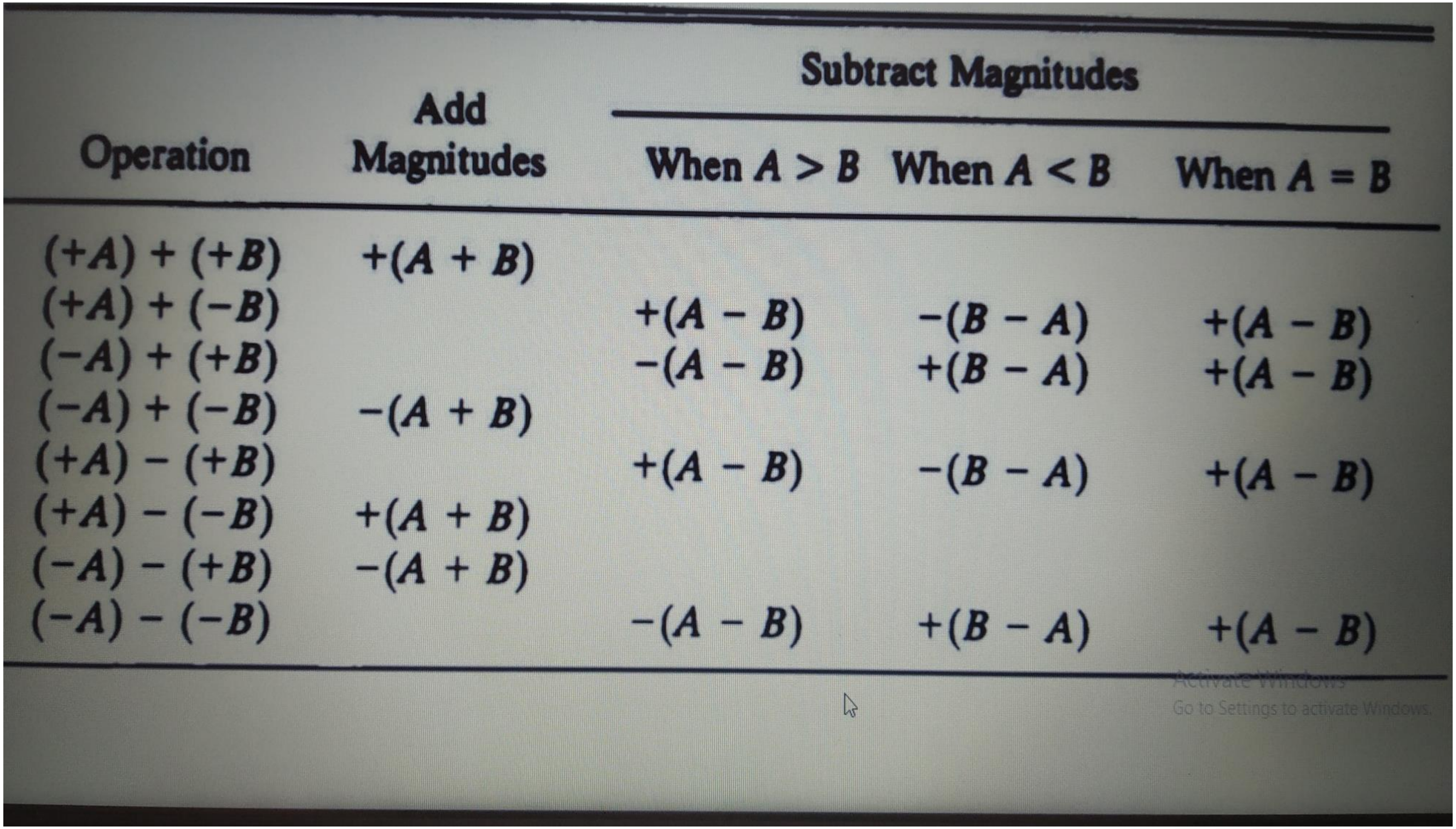
Introduction

- Algorithm can be defined as a finite number of well defined procedural steps to solve a problem. Usually, an algorithm will contain a number of procedural steps which are dependent on results of previous steps. A convenient method for presenting an algorithm is a flowchart which consists of rectangular and diamond –shaped boxes.

Addition and subtraction algorithm for signed-magnitude data

- Let the magnitude of two numbers be A & B. When signed numbers are added or subtracted, there are different conditions to be considered for each addition and subtraction depending on the sign of the numbers.
- The conditions are listed in the table.
- The table shows the operation to be performed with magnitude(addition or subtraction) are indicated for different conditions.

Conditions for addition and subtraction



Operation	Add Magnitudes	Subtract Magnitudes		
		When $A > B$	When $A < B$	When $A = B$
$(+A) + (+B)$	$+(A + B)$			
$(+A) + (-B)$		$+(A - B)$	$-(B - A)$	$+(A - B)$
$(-A) + (+B)$		$-(A - B)$	$+(B - A)$	$+(A - B)$
$(-A) + (-B)$	$-(A + B)$			
$(+A) - (+B)$		$+(A - B)$	$-(B - A)$	$+(A - B)$
$(+A) - (-B)$	$+(A + B)$			
$(-A) - (+B)$	$-(A + B)$			
$(-A) - (-B)$		$-(A - B)$	$+(B - A)$	$+(A - B)$

Addition Algorithm:

- When the signs of A and B are identical, add two magnitudes and attach the sign of A to the result.
- When the sign of A and B are different, compare the magnitudes and subtract the smaller number from the larger.
- Choose the sign of the result to be the same as A if A>B or the complement of sign of A if A < B.
- If the two magnitudes are equal, subtract B from A and make the sign of the result positive

Subtraction algorithm

- When the signs of A and B are different, add two magnitudes and attach the sign of A to the result.
- When the sign of A and B are identical, compare the magnitudes and subtract the smaller number from the larger.
- Choose the sign of the result to be the same as A if A>B or the complement of sign of A if A < B.
- If the two magnitudes are equal, subtract B from A and make te sign of the result positive.

Hardware Implementation

- Let A and B are two registers that hold the numbers.
- AS and BS are 2, flip-flops that hold sign of corresponding numbers. The result is stored In A and AS .and thus they form Accumulator register.
- We need to perform micro operation, A+ B and hence a parallel adder.
- A comparator is needed to establish if A> B, A=B, or A<B,
- We need to perform micro operations A-B and B-A and hence two parallel subtractor.
- An exclusive OR gate can be used to determine the sign relationship, that is, equal or not.
- Thus the hardware components required are a magnitude comparator, an adder, and two subtractors.

Hardware for signed-magnitude addition and subtraction

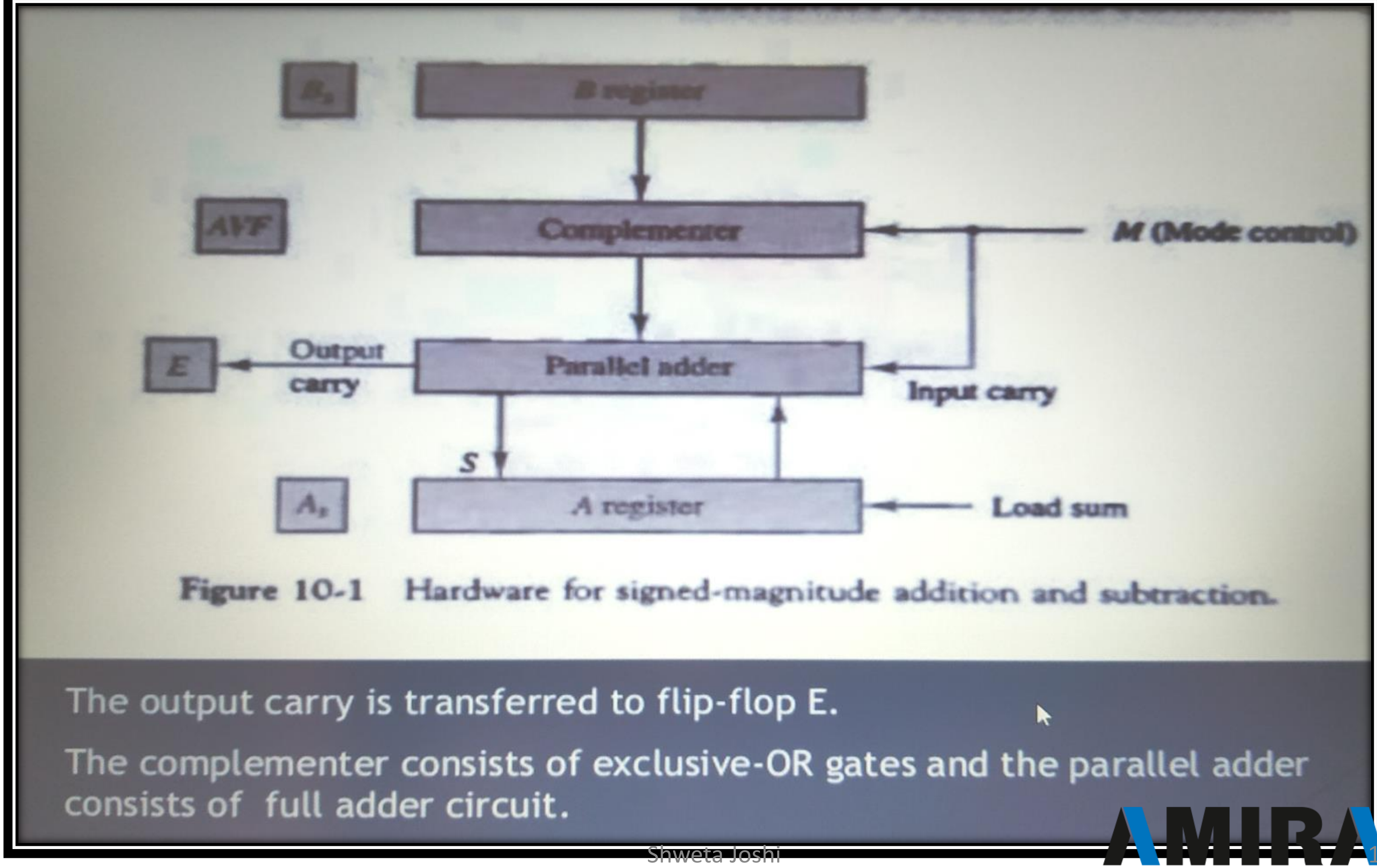


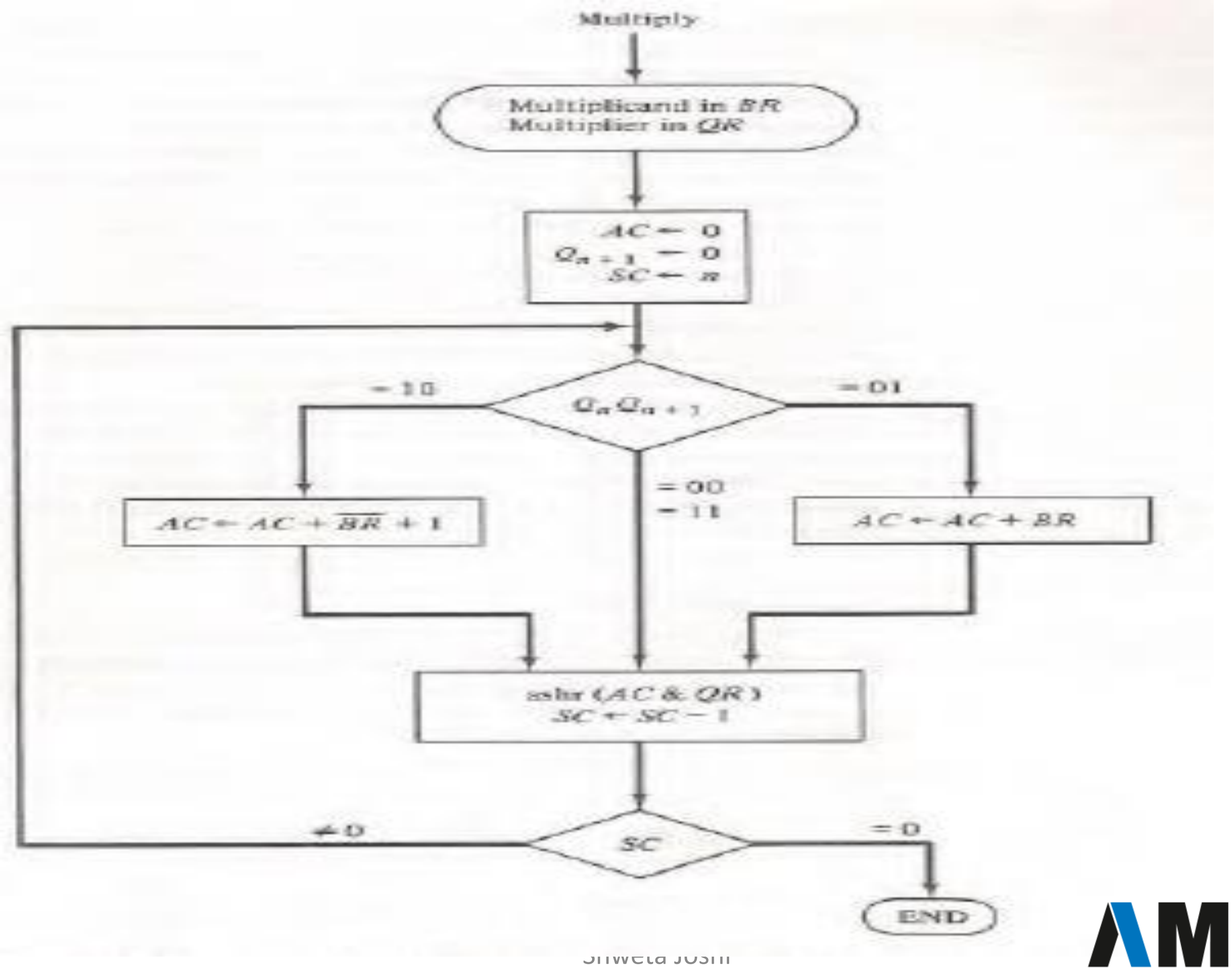
Figure 10-1 Hardware for signed-magnitude addition and subtraction.

The output carry is transferred to flip-flop E.

The complementer consists of exclusive-OR gates and the parallel adder consists of full adder circuit.

Booth Multiplication Algorithm

- Booth algorithm gives a procedure for multiplying binary integers in signed-2‘s complement representation. Refer flow chart here:

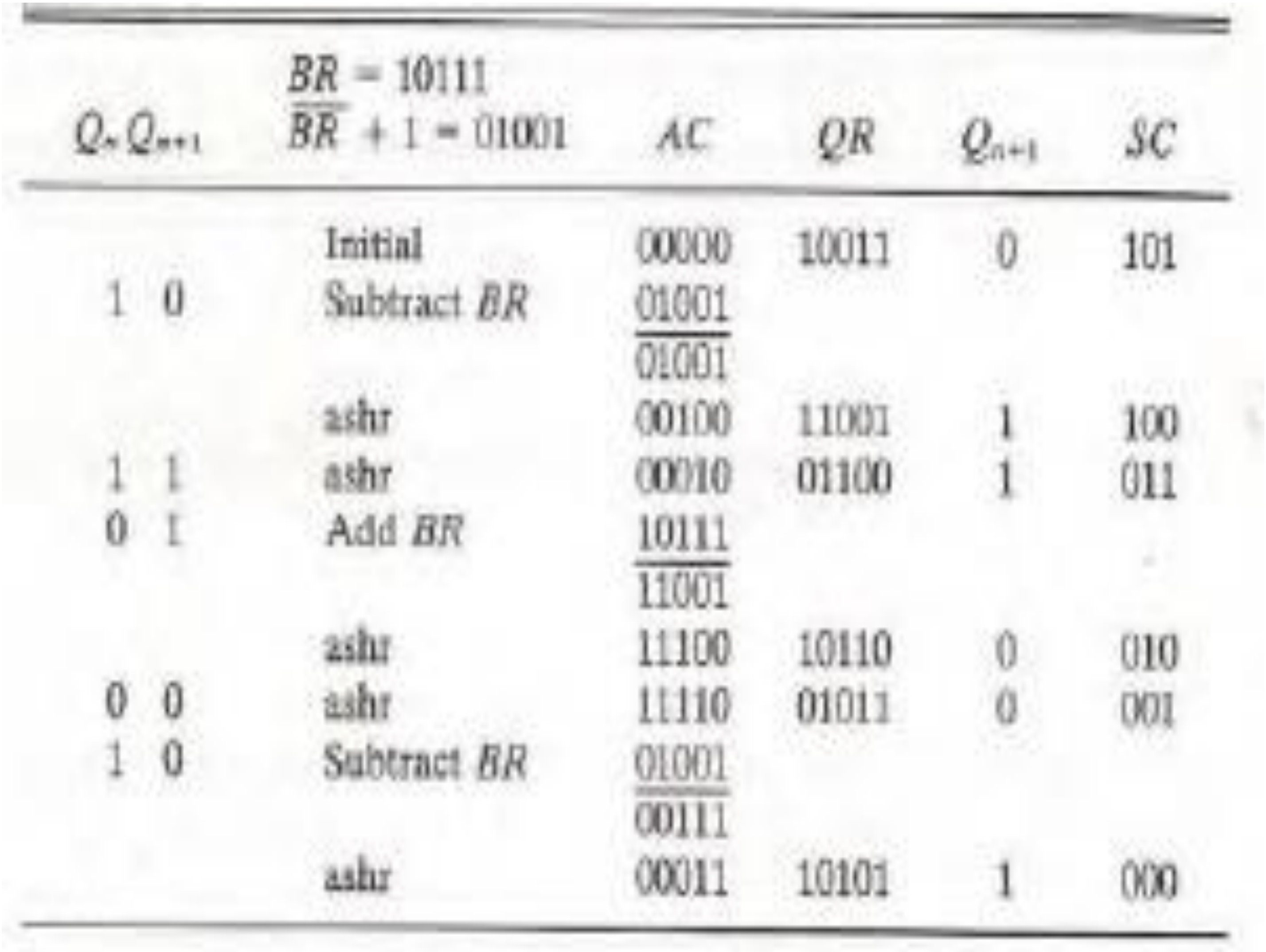


Booth Multiplication Algorithm

This table shows the step-by-step multiplication using BOOTH Algorithm Of:

(-9) x(-13)

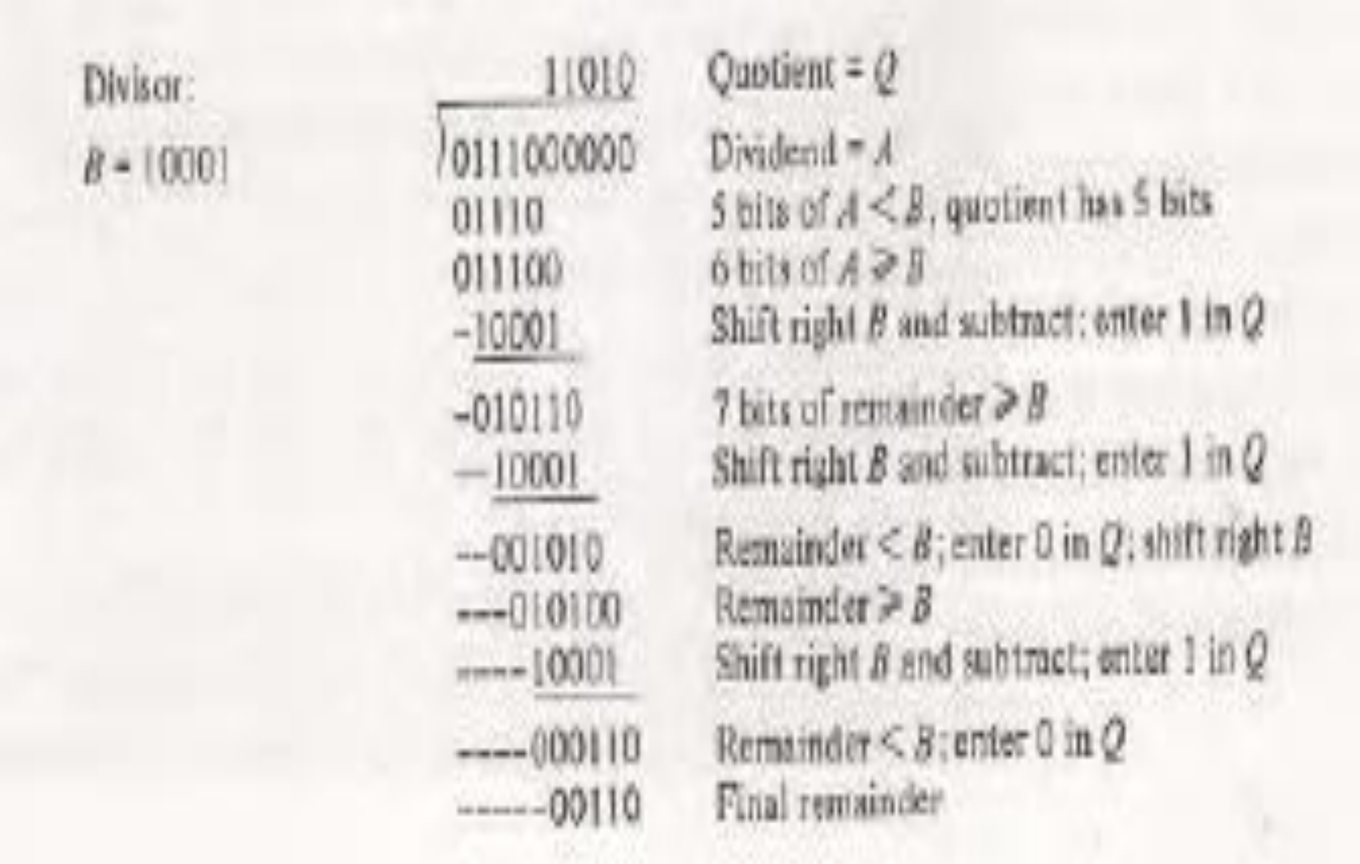
= +117.



$Q_n Q_{n+1}$	$BR = 10111$ $\overline{BR} + 1 = 01001$	AC	QR	Q_{n+1}	SC
	Initial	00000	10011	0	101
1 0	Subtract BR	01001			
		01001			
	ashr	00100	11001	1	100
1 1	ashr	00010	01100	1	011
0 1	Add BR	10111			
		11001			
	ashr	11100	10110	0	010
0 0	ashr	11110	01011	0	001
1 0	Subtract BR	01001			
		00111			
	ashr	00011	10101	1	000

Division Algorithm

Division of two fixed-point binary numbers in signed-magnitude representation is done with paper and pencil by a process of successive compare, shift, and subtract operations



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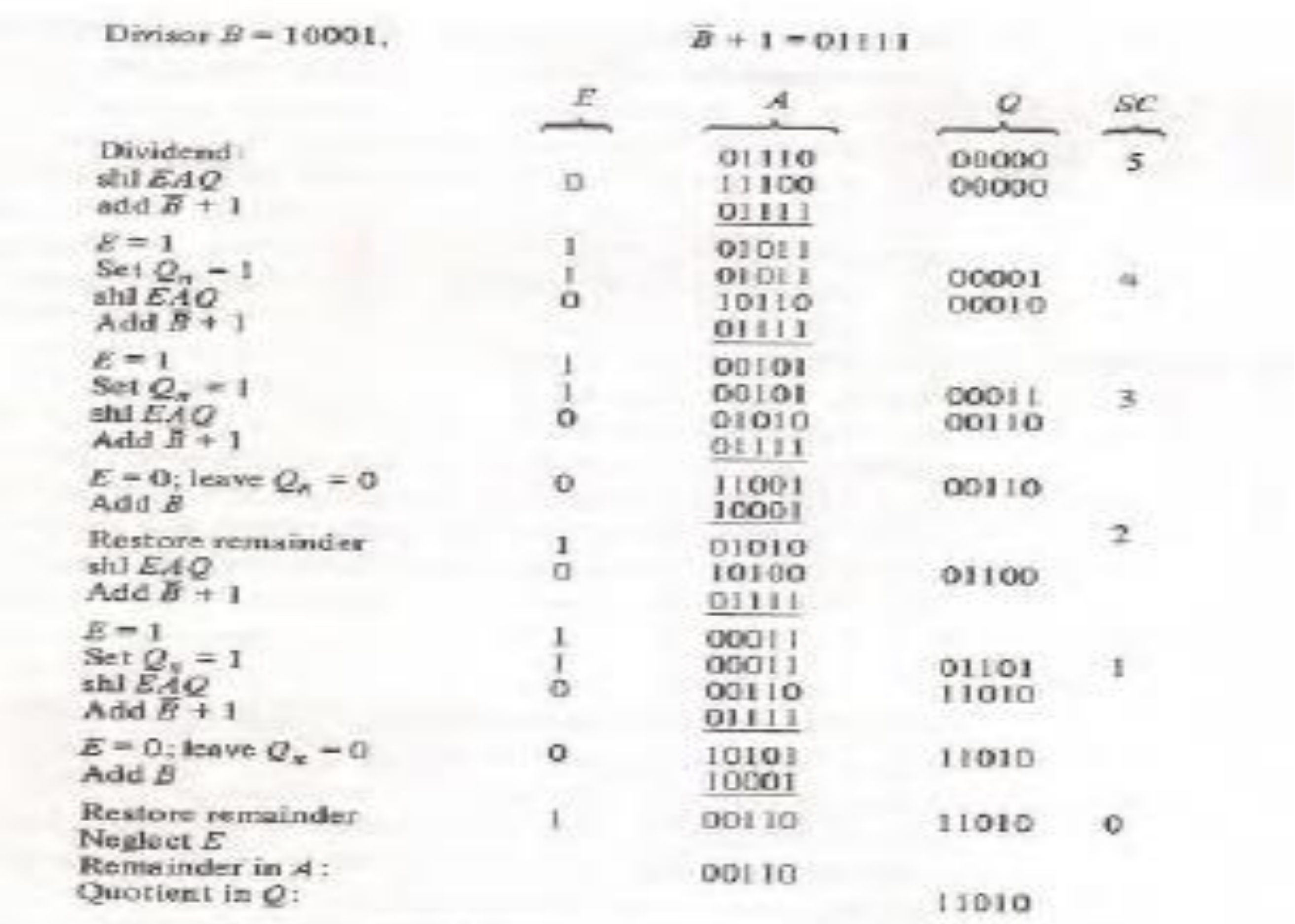
Divisor:                11010       Quotient = Q
B = 10001          ___________
                   )0111000000      Dividend = A
                    01110           5 bits of A < B, quotient has 5 bits
                    011100          6 bits of A ≥ B
                    -10001          Shift right B and subtract; enter 1 in Q
                    ______
                    -010110         7 bits of remainder ≥ B
                    —10001          Shift right B and subtract; enter 1 in Q
                     ______
                    --001010        Remainder < B; enter 0 in Q; shift right B
                    ---010100       Remainder ≥ B
                    ----10001       Shift right B and subtract; enter 1 in Q
                        ______
                    ----000110      Remainder < B; enter 0 in Q
                    -----00110      Final remainder
```

Division Algorithm

Example of binary division with digital hardware

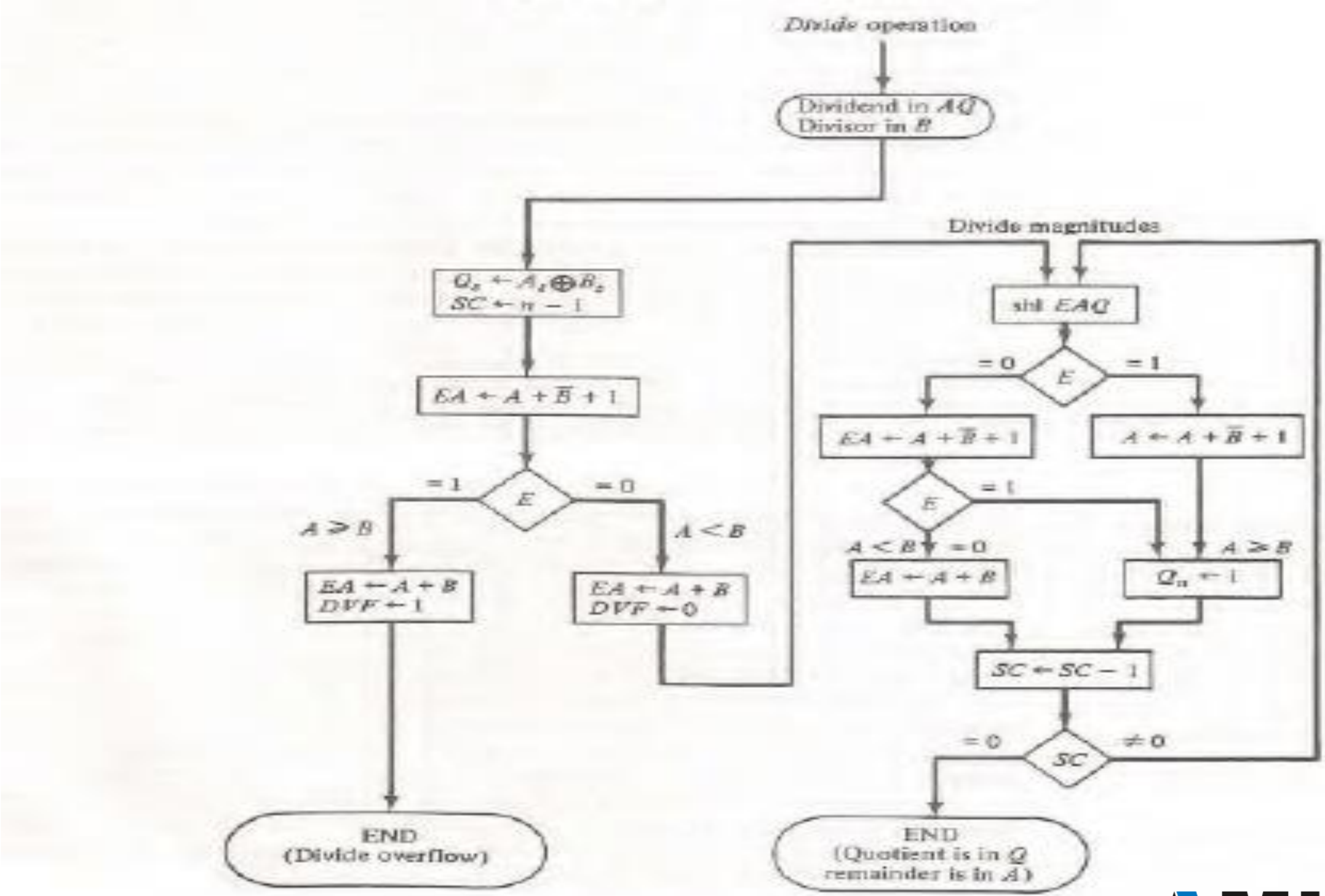


Divisor $B = 10001$, $\bar{B} + 1 = 01111$

	E	A	Q	SC
Dividend:		01110	00000	5
shl EAQ	0	11100	00000	
add $\bar{B} + 1$		01111		
$E = 1$	1	01011		
Set $Q_n = 1$	1	01011	00001	4
shl EAQ	0	10110	00010	
Add $\bar{B} + 1$		01111		
$E = 1$	1	00101		
Set $Q_n = 1$	1	00101	00011	3
shl EAQ	0	01010	00110	
Add $\bar{B} + 1$		01111		
$E = 0$; leave $Q_n = 0$	0	11001	00110	
Add B		10001		
Restore remainder	1	01010		2
shl EAQ	0	10100	01100	
Add $\bar{B} + 1$		01111		
$E = 1$	1	00011		
Set $Q_n = 1$	1	00011	01101	1
shl EAQ	0	00110	11010	
Add $\bar{B} + 1$		01111		
$E = 0$; leave $Q_n = 0$	0	10101	11010	
Add B		10001		
Restore remainder	1	00110	11010	0
Neglect E				
Remainder in A:		00110		
Quotient in Q:			11010	

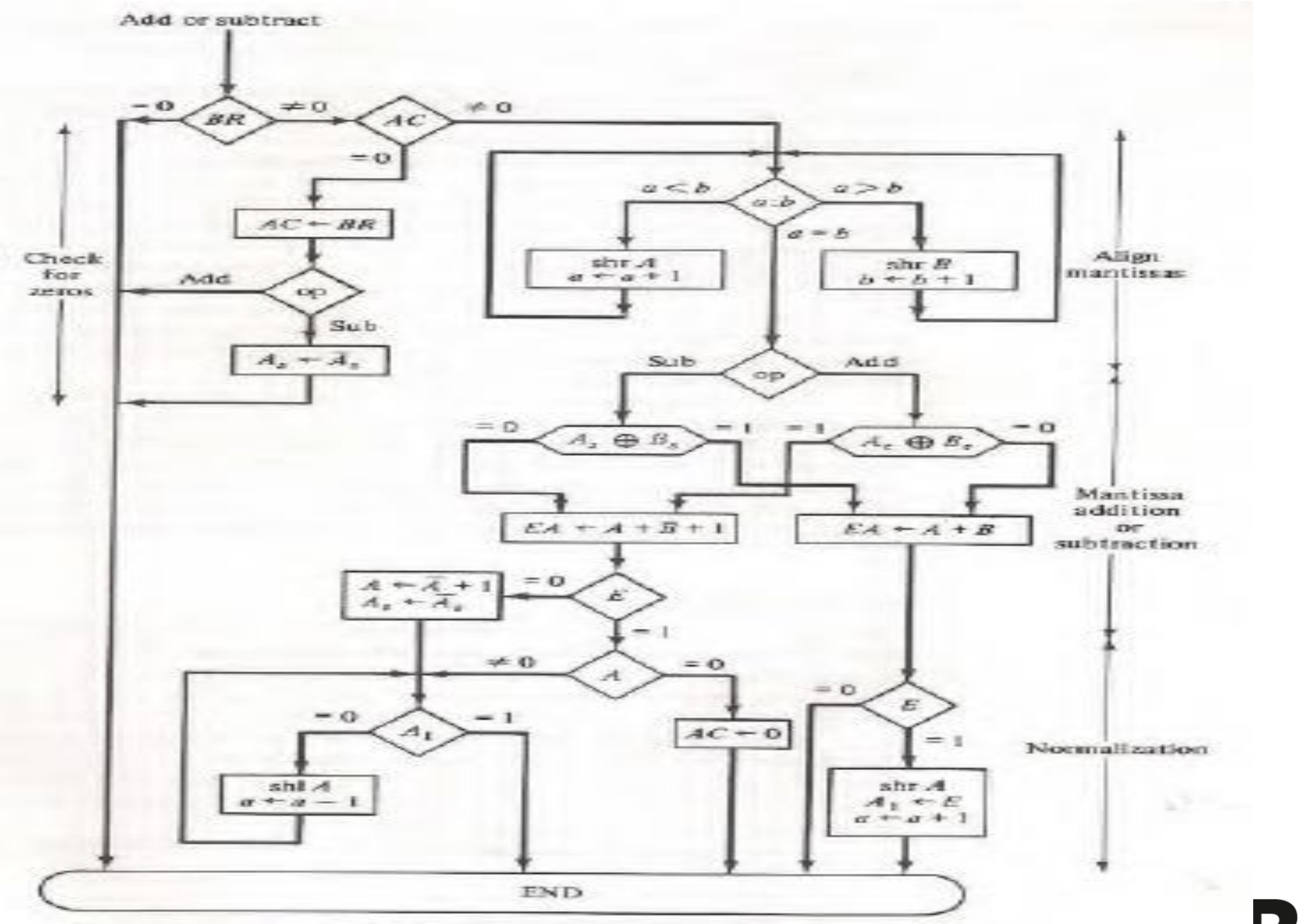
Division Algorithm

Flowchart for divide operation



Floating point Arithmetic operations

- Addition and subtraction of floating point numbers

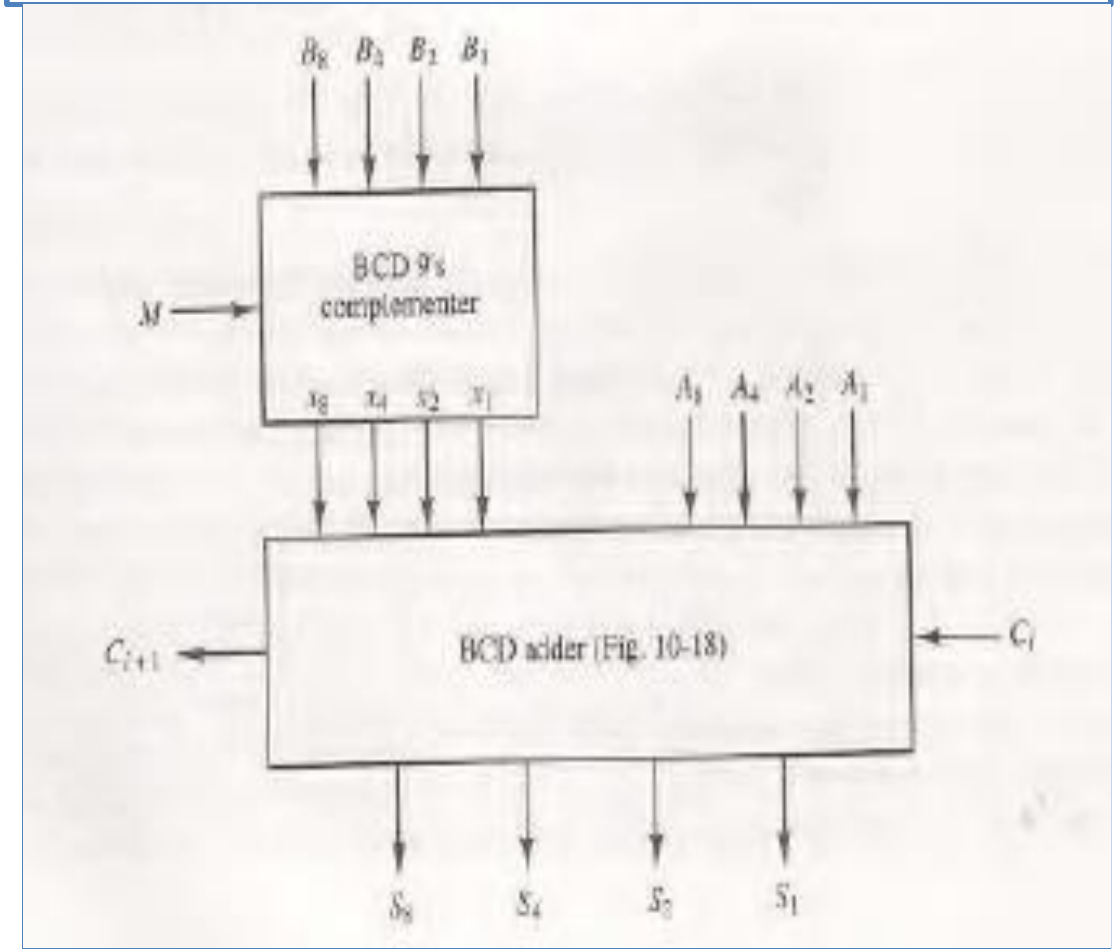


Decimal Arithmetic Unit

- The user of a computer prepares data with decimal numbers and receives results in decimal form.
- Electronic calculators use an internal decimal arithmetic unit since inputs and outputs are frequent.
- A decimal arithmetic unit is a digital function that performs decimal microoperations.
- It can add or subtract decimal numbers, usually by forming the 9's or 10's complement of the subtrahend.
- The unit accepts coded decimal numbers and generates results in the same adopted binary code.
- A single-stage decimal arithmetic unit consists of nine binary input variables and five binary output variables, since a minimum of four bits is required to represent each coded decimal digit.
- Each stage must have four inputs for the augend digit, four inputs for the addend digit, and an input-carry. The outputs include four terminals for the sum digit and one for the output-carry

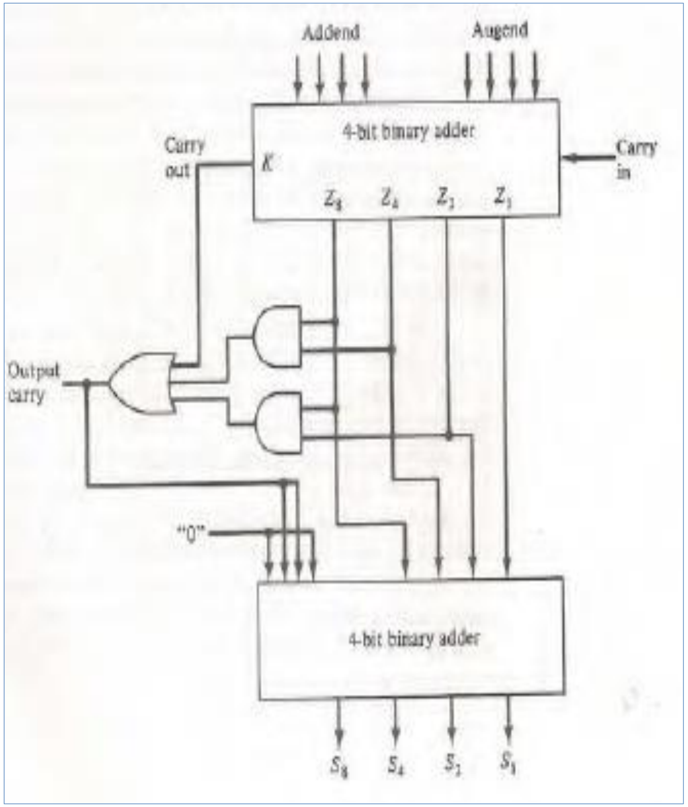
Decimal Arithmetic Unit

- One stage of Decimal arithmetic unit



BCD ADDER

BCD adder is a circuit that adds two BCD digits in parallel and produces a sum digit also in BCD.



References

- **Images , descriptive Tables , from Computer System Architecture, Morris Mano, 3rd edition Prentice Hall**

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